The ESO Infrared Detector High-Speed Array Control and Processing Electronics IRACE

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Abstract

The ESO Infrared Detector High Speed Array Control and Processing Electronics, IRACE, is designed as a modular system which supports readout and data processing of arrays with four, and eventually more, output channels. In addition, the system can handle several separate arrays by routing the data to multiple processing chains. Detector front-end(s) are galvanically isolated from the data processing and system administration by fiberoptic links. The multiprocessor system(s) for on-line data handling are based on the IMS T9000 transputer, the most advanced European-produced processor. A key component of the whole system is a 1 Gigabit/s fiberoptic link. The link not only transmits data, but the architecture of the system allows distribution of data to the multiprocessor system(s) in a flexible and simple way. We present here the principles of the system operation, the achieved readout and on-line processing speeds and present first measurement results with a 1024 × 1024 pixel IR array.

Introduction

The electronic part of the data-acquisition system IRACE consists of the detector front-end and a data-acquisition computer or multiprocessor system for more demanding applications. The low-noise detector front-end and the data-acquisition computer are galvanically isolated, to avoid ground loops. An additional advantage of fiberoptics is the ability to transmit data over huge distances at high speed, e.g. between telescope and control room.

The ESO IR data-acquisition system IRACE is primarily built for the VLT instrument ISAAC, which will be equipped with a 4-output channel 256 × 256 or, if available, 32-output channel 1024 × 1024 pixel InSb array in its long-wavelength channel from 2.5 to 5 µm and a MCT 1024 × 1024 array for the short wavelength channel from 1 to 2.5 µm. The data transmission between detector front-end and data-acquisition computer system requires a high speed link, e.g. for double-correlated sampling in the L filter (3.8 µm) with a scale of 0.23″/pixel, we expect a flux of 1.84E06 photons/s/pixel (based on measurements with the ESO IRAC1 camera at the 2.2-m telescope). That gives a data rate of ∼ 4E08 bits/s or 180 GByte/h for 16 bit ADC's
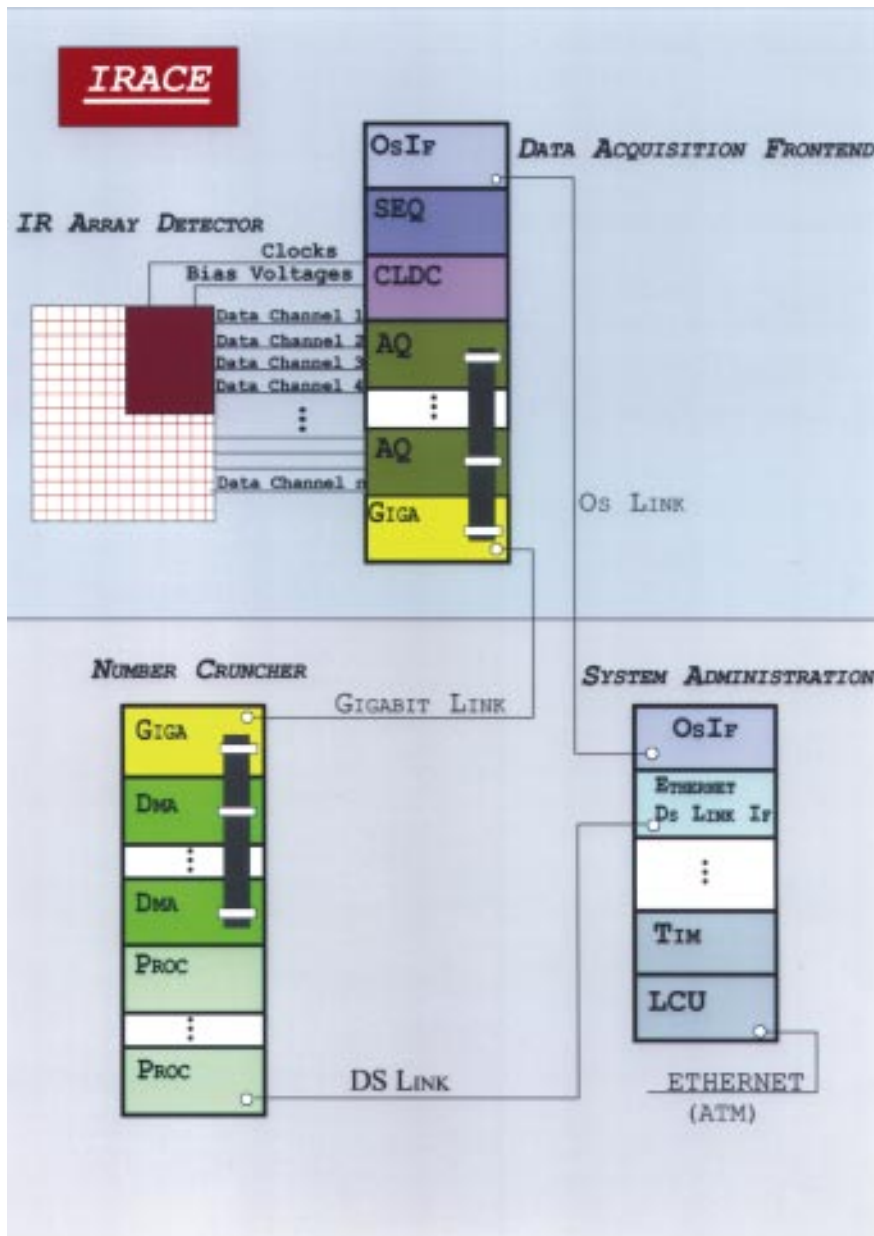

Figure 1: IRACE Block Diagram.

Figure 2: IRACE.

and an array with 32 parallel output channels. This shows that pre-processing of the incoming data is absolutely necessary. But even in the low background bands J, H and K multiple, non-destructive sampling and linear regression analysis gives the best results at short readout times per frame with correspondingly high frame and data rates. To process in real time the continuous stream of data, a multiprocessor system based on T9000 transputers and C104 packet switches was developed. The system is scaleable to the processing needs and the use of OCCAM as programming language, and the INMOS software tools are very convenient for multiprocessor system programming.

The IRACE System

Figure 1 shows a block diagram of IRACE and Figure 2 a photograph of the system, which consists of four main groups:
- The IR array detector with differential drivers on the detector data lines
- The Data Acquisition Front-end
- The Number Cruncher
- The System Administration

The IR array detector is located inside a vacuum vessel and the analogue signals are fed out over differential line drivers to the data terminal. Two additional terminals on the vessel supply the clock and bias voltages.

The data-acquisition front-end is a VME-size crate located on the vacuum vessel. It contains the clock pattern sequencer (SEQ), the clock and bias generator (CLDC), the acquisition modules (AQ), the fiberoptic link interface to the system administration (OsIf) and the fiberoptic high-speed data link (GIGA). The front-end is a T8 transputer system, programmed and set up by OsIf, a T8 protocol fiberoptic link. The sequencer is FIFO based and supports 48 bit wide words with a cycle time > 33 ns. The module with the level converters for the clocks and the bias generators (CLDC) provides 16 clocks and 16 biases. All voltage levels are set by software and can be inspected with a telemetry system at any time, even during detector readout. The differential analogue data lines are fed into a four-channel analogue to digital converter board (AQ) with preamplifiers and anti-aliasing filters. The digitised data leave AQ to a high speed bus (~100 MByte/s) and enter the transmitter side of the Gigabit fiberoptic link (GIGA). The data leave the front-end over a high-speed fiberoptic link with 1Gbit/s. Front-end and array detector are galvanically completely floating, so it is possible to choose a ground point on the instrument without danger of creating ground loops.

The System Administration and the Number Cruncher reside in another VME crate. This crate may be installed
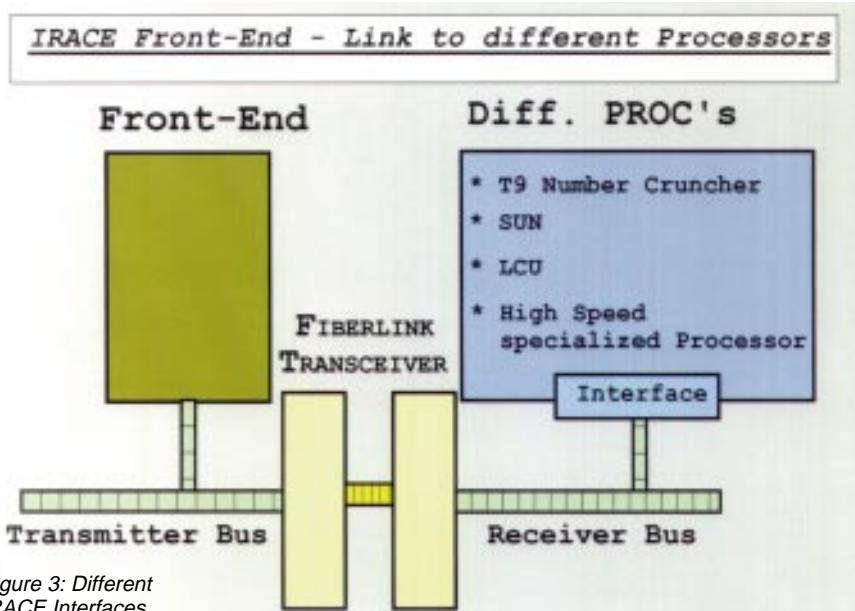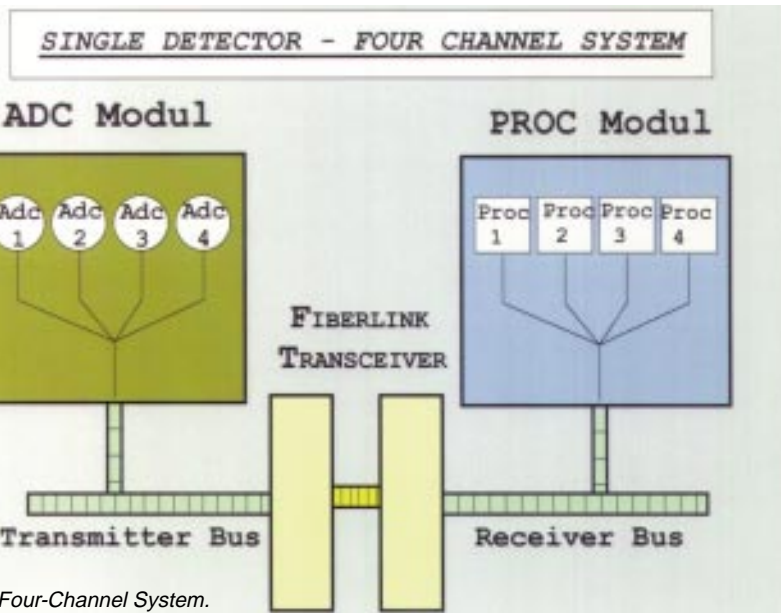

Figure 3: Different IRACE Interfaces.
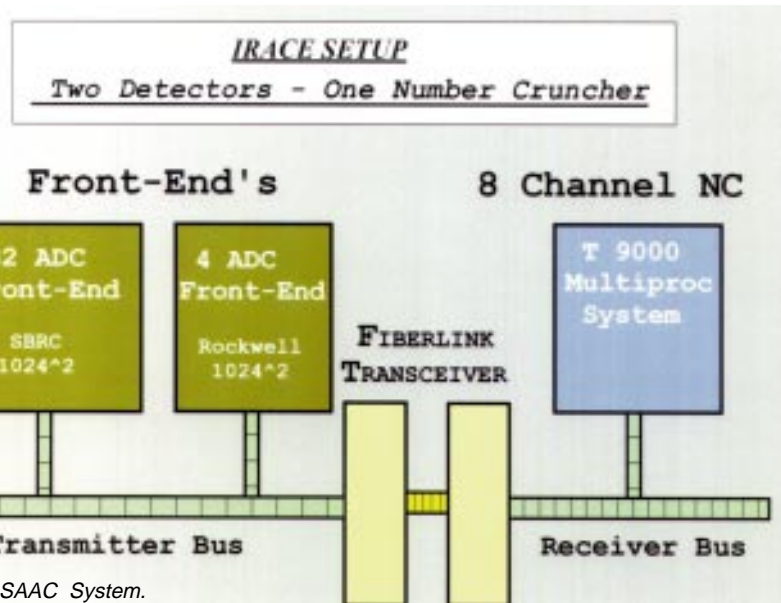

Figure 4: Four-Channel System.
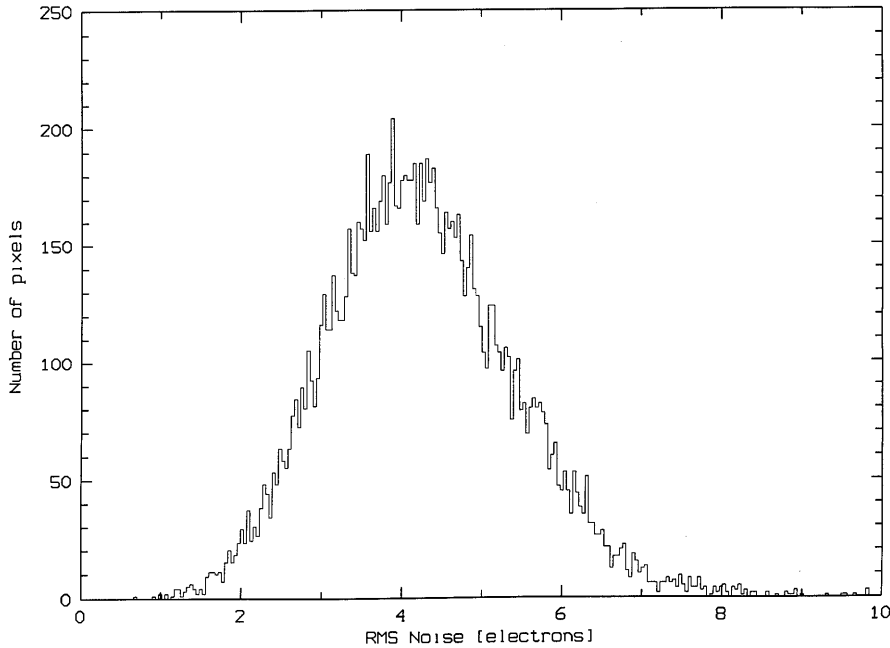

Figure 5: ISAAC System.

Figure 6: Noise Histogram of the HAWAII 1024 × 1024 MCT array.

in a remote location; the only physical connection to the front end is by the fiberoptic links. Link lengths up to 2 km are possible. The System Administration consists of the Ethernet (or possibly an ATM) interface to the host workstation, the local control unit (LCU), the time reference system (TIM), the T8 Os fiberoptic link to the front-end (Oslf), and an Ethernet DS link interface to the number cruncher. All downloading, commands and housekeeping operations are done over this system.

The number cruncher system gets the data from the receiver of the Gigabit fiberoptic transceiver (GIGA). The fiberoptic link receiver puts the data onto a high-speed bus with identical protocol and function as the bus on the front-end side. Dma controllers (DMA) on this bus transport and interface the incoming data to the multiprocessor system (PROC). While data are being processed in real time, intermediate and averaged images are sent to the LCU and to the host workstation. It is possible to have an optional connection on the number cruncher to an array of SCSI disks for raw data taking and a fast on line display.

Functionally there are two blocks, the detector control block and the data-acquisition chain. The detector control block consists of sequencer and clock/bias driver which are responsible for the set-up of the detector itself. The acquisition chain starts at the ADC's of AQ and includes the high-speed fiberoptic link and the number cruncher. The only direct link between the two blocks is the conversion signal produced by the sequencer. The two blocks can be seen as independent systems which simplifies testing and maintenance because both blocks can run independently.

A completely new method was developed for the data-acquisition chain to fulfil the high-speed requirements of the new IR arrays with multiple outputs (up to 32 at present) and the corresponding high data rates. This system is centred around a 1 Gigabit/s fiberoptic link. The fiberoptic link can be interfaced to different platforms. For applications where number crunching is not required, the gigabit link can be directly interfaced to the

LCU or any processor system (Fig. 3). The multiprocessor system built for ISAAC is based on T9000 transputers and C104 packet routing switches. The number cruncher is a modular design and can be tailored to the needs of the application and the required speed of readout and data processing.

The gigabit link connects the ADC's to the number cruncher system. The link not only transmits data but also distributes the data directly to the input processors of the number cruncher system. In Figure 4, the data of a 4-channel detector (like the Rockwell HAWAII 1024 × 1024 in ISAAC) are routed to a four-channel number cruncher front-end. Each quadrant is routed to one input processor. For detectors with multiple output channels (like the SBRC ALADDIN 32-channel 1024 × 1024 InSb array) more computing power is required. In this case the ADC module consists of 32 ADC's. On the processor side, an 8-input channel front-end has to be implemented with each input processor this is processing 4 detector channels.

Two detectors are installed in ISAAC; a 4-channel Rockwell 1024 × 1024 for the wavelength range from 1 to 2.5 μm and a SBRC 1024 × 1024 for the 2.5 to 5 μm region. Only one arm of the instrument is active for a given observation. IRACE is able to process the two different detectors with only one number cruncher, because the system can be dynamically configured to the active detector system (Fig. 5).

Supported Data Processing Modes and Achieved Readout Speeds

The following readout modes have been implemented:
• Uncorrelated sampling
• Double-correlated sampling
• Triple-correlated sampling
• Multiple non-destructive readout with linear fitting of the integration ramp
• On-chip tip tilt correction with destructive readout
• On-chip tip tilt correction with non-destructive readout

TABLE 1. Readout speed of IRACE.

READ MODE	READ + PROCESSING TIME per PIXEL and CHANNEL TIME (ns)	READOUT TIME 4 Channel IRACE 4 Channel HAWAII TIME (ms)	READOUT TIME 8 Channel IRACE 32 Channel ALADDIN TIME (ms)
RAW	300	80 + Reset	40 + Reset
RAW + SUM	300	80 + Reset	40 + Reset
DOUBLE	600	160 + Reset	80 + Reset
DOUBLE + SUM	600	160 + Reset	80 + Reset
NON-DESTRUCTIVE	750	200 + Reset	100 + Reset

Reset = 2 ms
Non-Destructive Readout includes time for linear fit of consecutive reads.

- Raw data taking with high storage of individual readouts to local SCSI disk array

Processing Time for Different Read Modes per Pixel and Channel

In Table 1, the read and processing time of IRACE is shown. Column 1 describes the read mode, column 2 shows the read and processing times for a single pixel in one channel, Column 3 the possible time for readout of a 4-channel detector like the Rockwell 1024 × 1024 HAWAII array and Column 4 shows the time for readout with an 8-channel IRACE system as used with the SBRC ALADDIN 1024 × 1024 InSb array. The fastest readout speed per pixel which is possible with the HAWAII detector was measured to be 3 μs/pixel corresponding to an array readout time of 800 ms. IRACE is a factor of four faster than the analogue bandwidth of this array. In the case of the ALADDIN 1024^2 array with 32 parallel outputs and 3μs/pixel, an 8-channel system just matches the speed requirements of 100 ms for the most demanding processing task of multiple non-destructive readout.

For a window of 256 × 256 pixels applying multiple non-destructive readouts and a least-square fit of the integration ramp, the obtained noise histogram is shown in Figure 6. The noise histogram peaks at 4 electrons rms. The conversion of ADU's to electrons was calibrated by the usual shot noise method. To compare this noise figure with the common definition of readout noise per single readout as defined for double correlated sampling, it has to be divided by the square root of 2 and corresponds to an rms noise of 2.8 electrons. This is the best noise figure ever reported for IR arrays

We could also demonstrate the IRACE system performance to detect a very faint thermal target. Figure 7 shows the K prime image of a thermal bar pattern at ambient temperature taken with a good quadrant of the HAWAII engineering grade array. The temperature difference of the bars is 4.0 10^{-2} K. A cryogenic neutral-density filter was used to attenuate this pattern by a factor of 10^{-2} to simulate the low background in the spectroscopic mode of ISAAC. The image is a raw difference with the target shifted in position. The bar pattern at the bottom edge of the image is at the detection limit. The contrast of the pattern corresponds
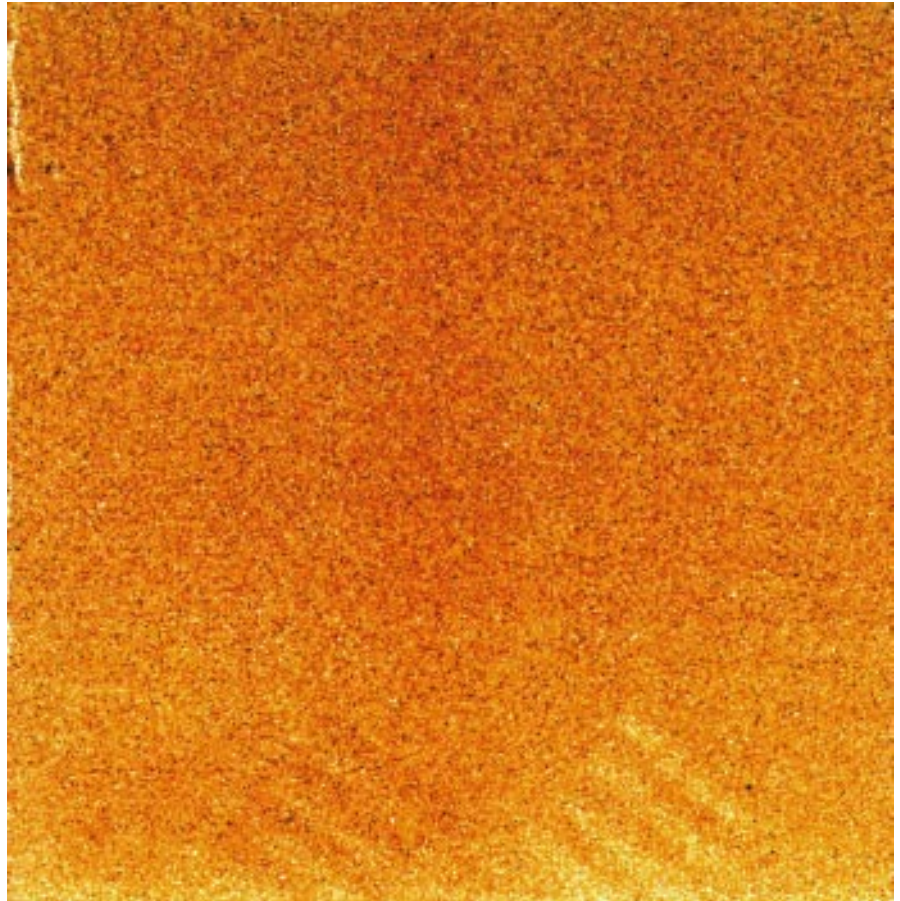

Figure 7: Faint thermal target at bottom edge of the image taken with one quadrant of the HAWAII 1024 × 1024 MCT array. The contrast of the thermal target corresponds to a signal of 6 electrons during an integration time of 2 minutes.

to a signal of 6 electrons per pixel integrated in a two-minute exposure. The detected photon-generated current is 5 10^{-2} electrons/sec which well demonstrates the performance of IRACE.

Conclusions

The ESO Infrared Detector High Speed Array Control and Processing Electronics IRACE is a flexible and modular system for high-speed and low-noise data acquisition. With its huge and scaleable computing power, it fulfils the requirements for future detector developments. A big advantage is the use of T9000 transputers with their inherent communication capabilities and large memory sizes. The system is completely programmable in the high-level language OCCAM, which simplifies parallel

processing. First test results with a 1024 × 1024 IR array detector have yielded a read noise of 4 e$^-$ and detection of a signal corresponding to only 6 e$^-$ during an integration time of 2 minutes. We conclude that the astronomical performance of ISAAC will be limited by detector and/or background noise and not by the IRACE acquisition system.

Acknowledgements

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