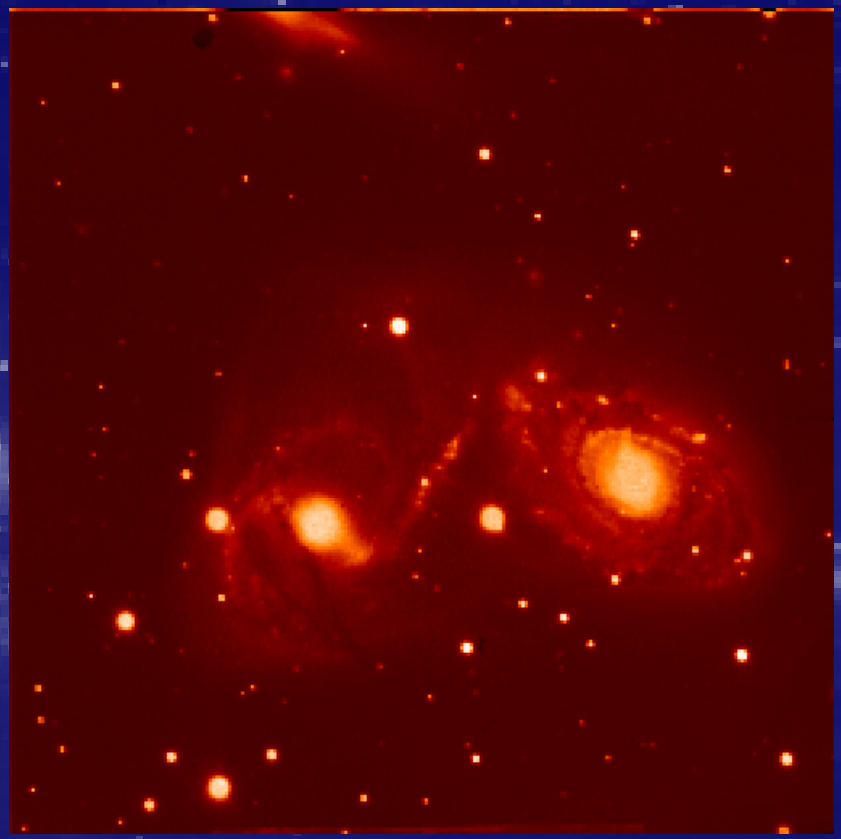
NGC

Detector Array Controller Based on High Speed Serial Link Technology



First Light

PICNIC Array Mux

Image of ESO Messenger Front Page

M.Meyer
July 08

Conventional Approach : Acquisition System (IRACE)

IRACE Back-end

PCI Interface

IRACE Front-end

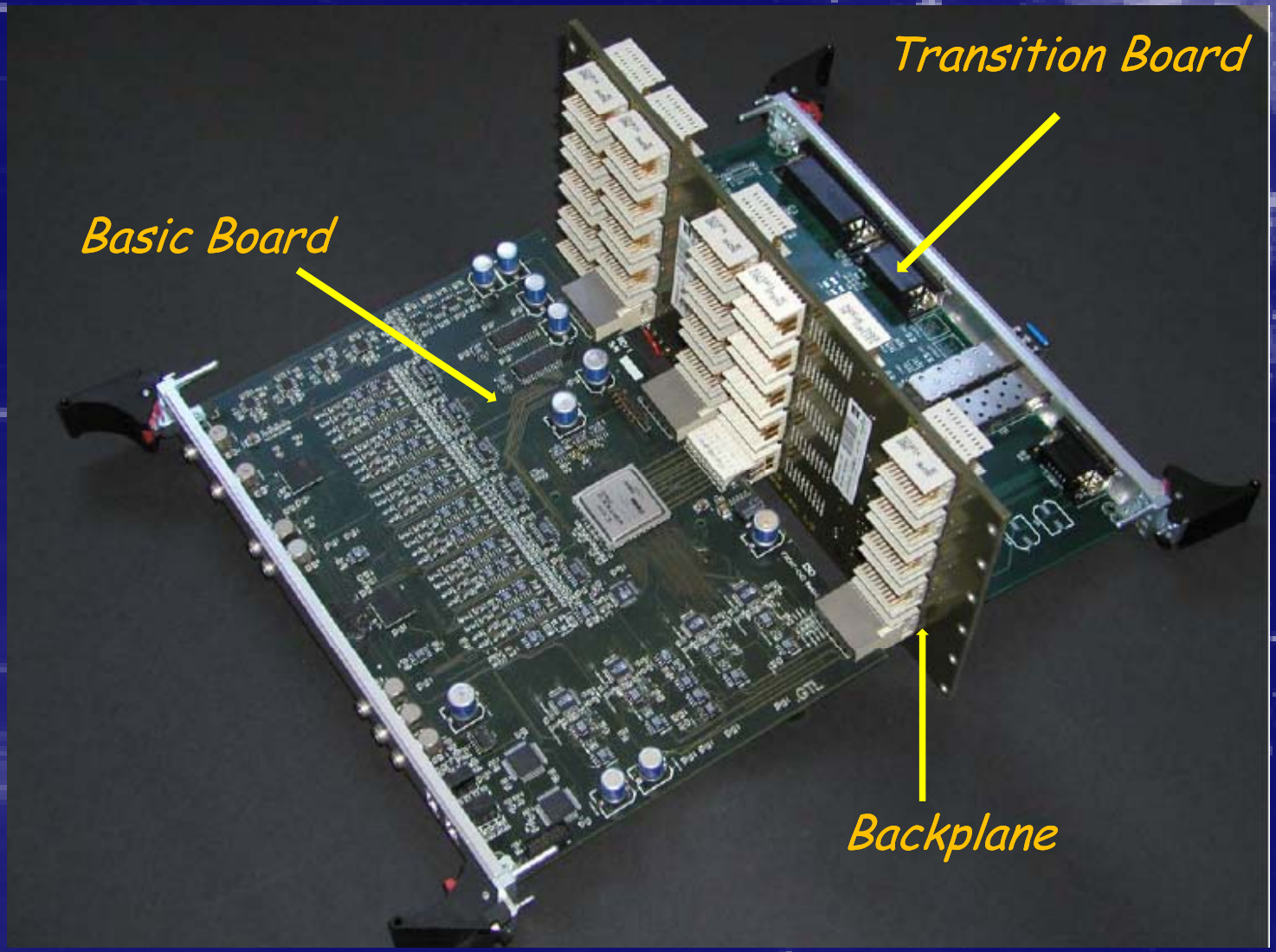
Communication and Data Transfer

Acquisition Module(s)

Sequencer

Clock and Bias

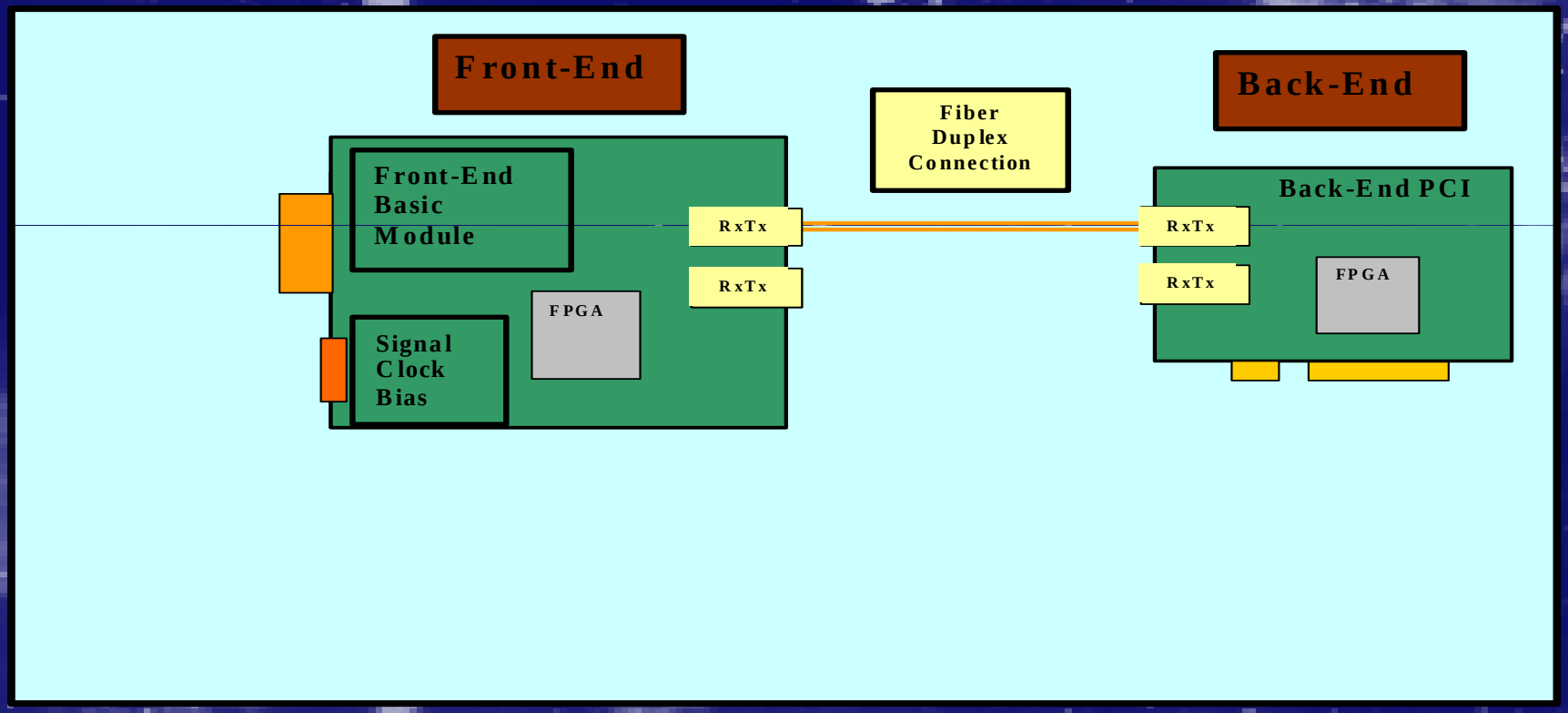
NGC Front-end
(Shown: Complete 4 Channel System)



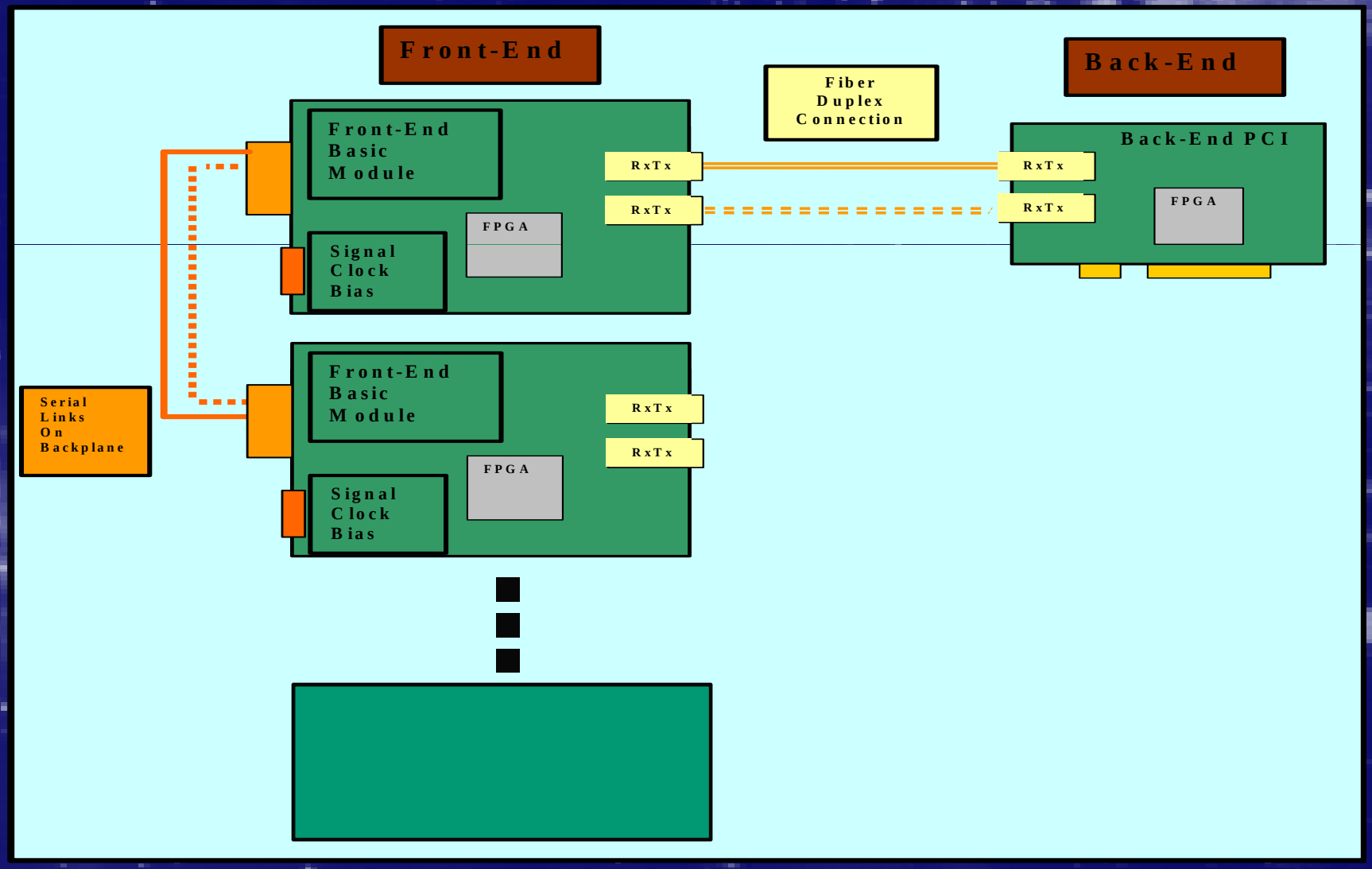
NGC System

- NGC is designed as a modular system consisting mainly of a PCI Back-end, a Front-end unit, detector preamplifiers and a remotely located power supply.
- There is no processor, no parallel inter-module data bus on the front-end side. Advanced FPGA link technology is used to replace conventional bus logic.
- Connection between Back and Front-end only by fibers with high speed links (200MB/s).
- Connection between Front-end modules with high speed copper links (200MB/s).
- Low noise achieved for IR detectors and CCD's
- No disturbance from digital logic detected
- Power Consumption on a four channel Front-end is ~ 12 Watts
- A four channel Front-end system does not require active cooling.

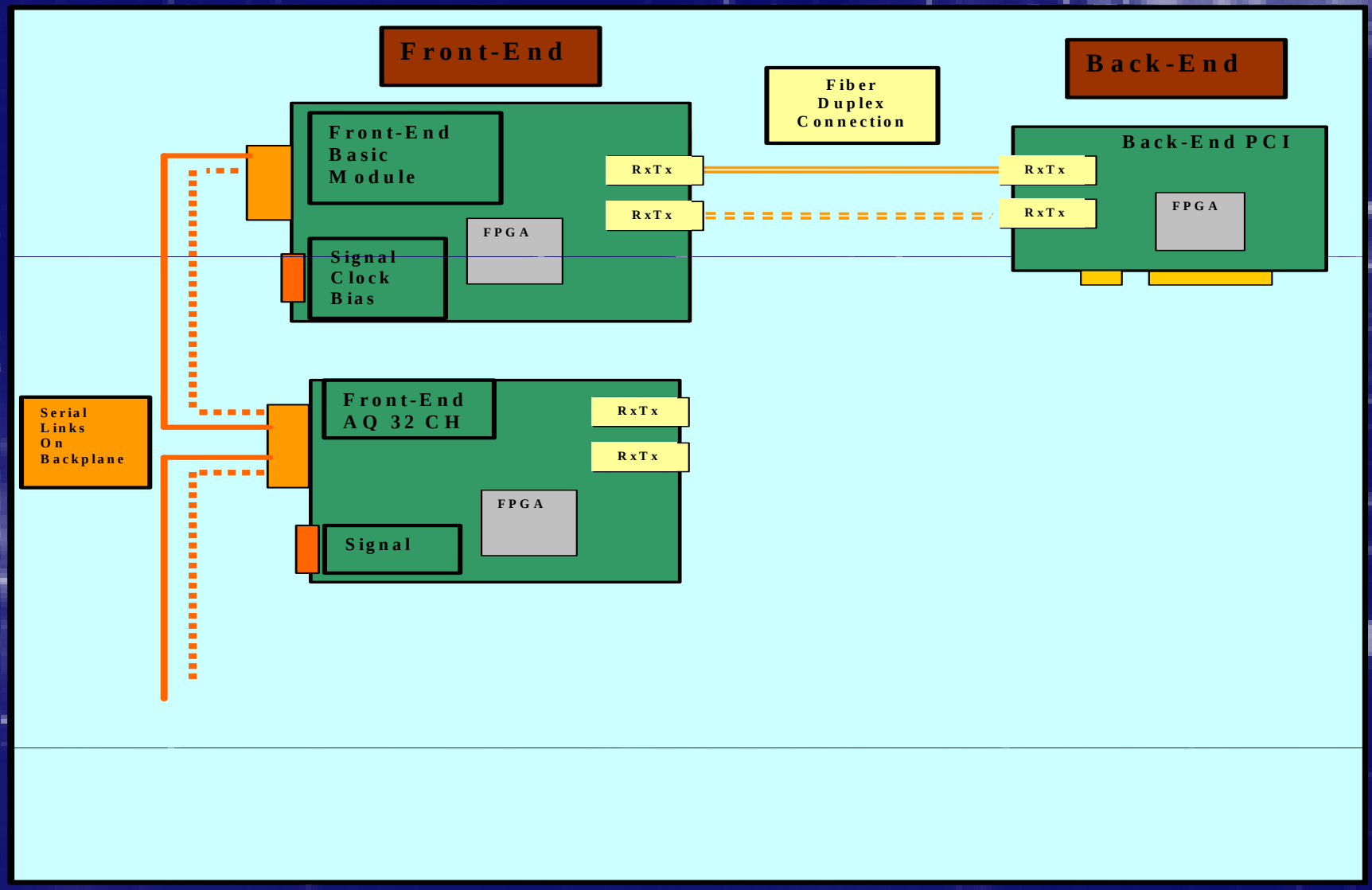
Basic System



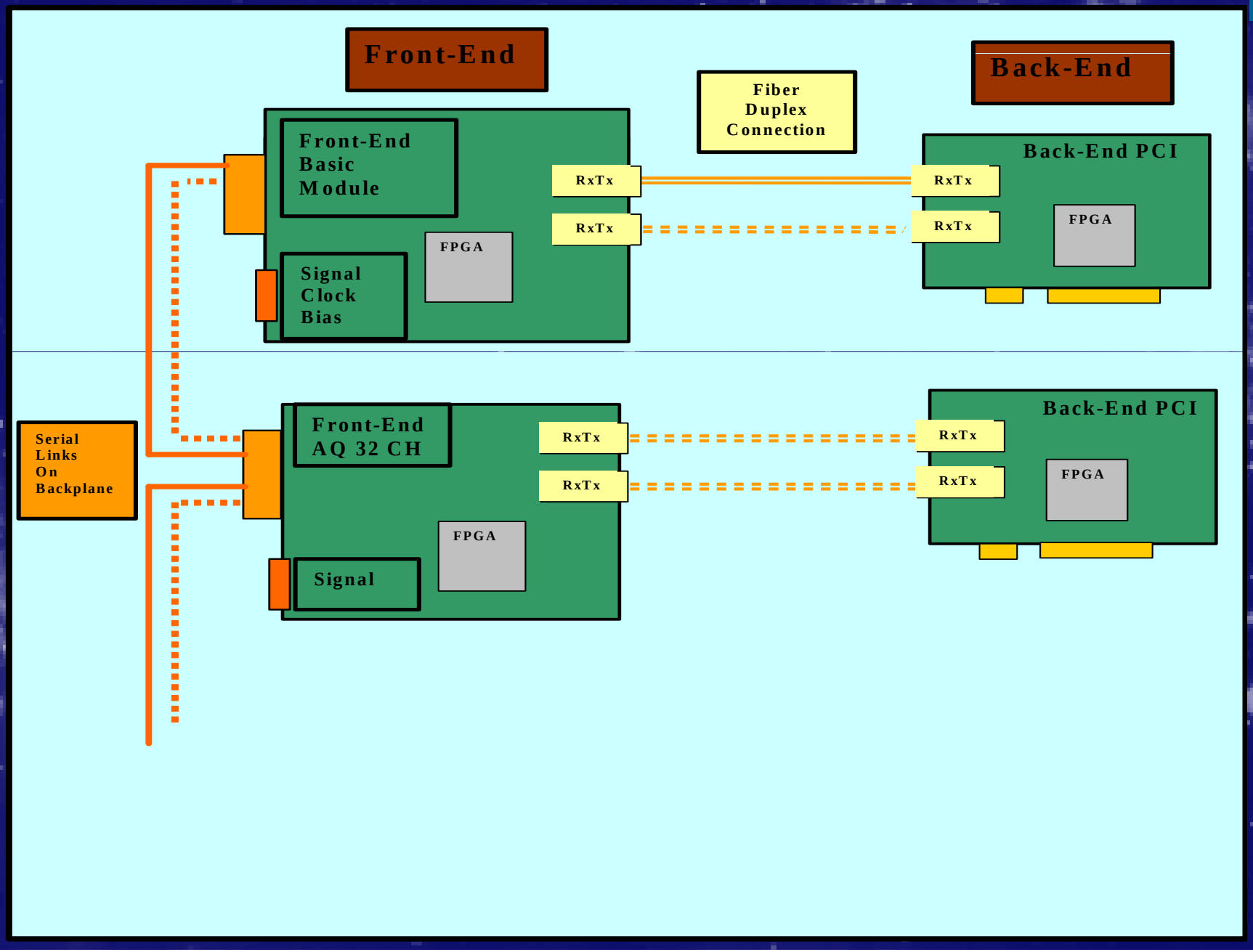
Synchronized Read-out of more than one Detector Application : MUSE– Six CCD Controllers per DFE



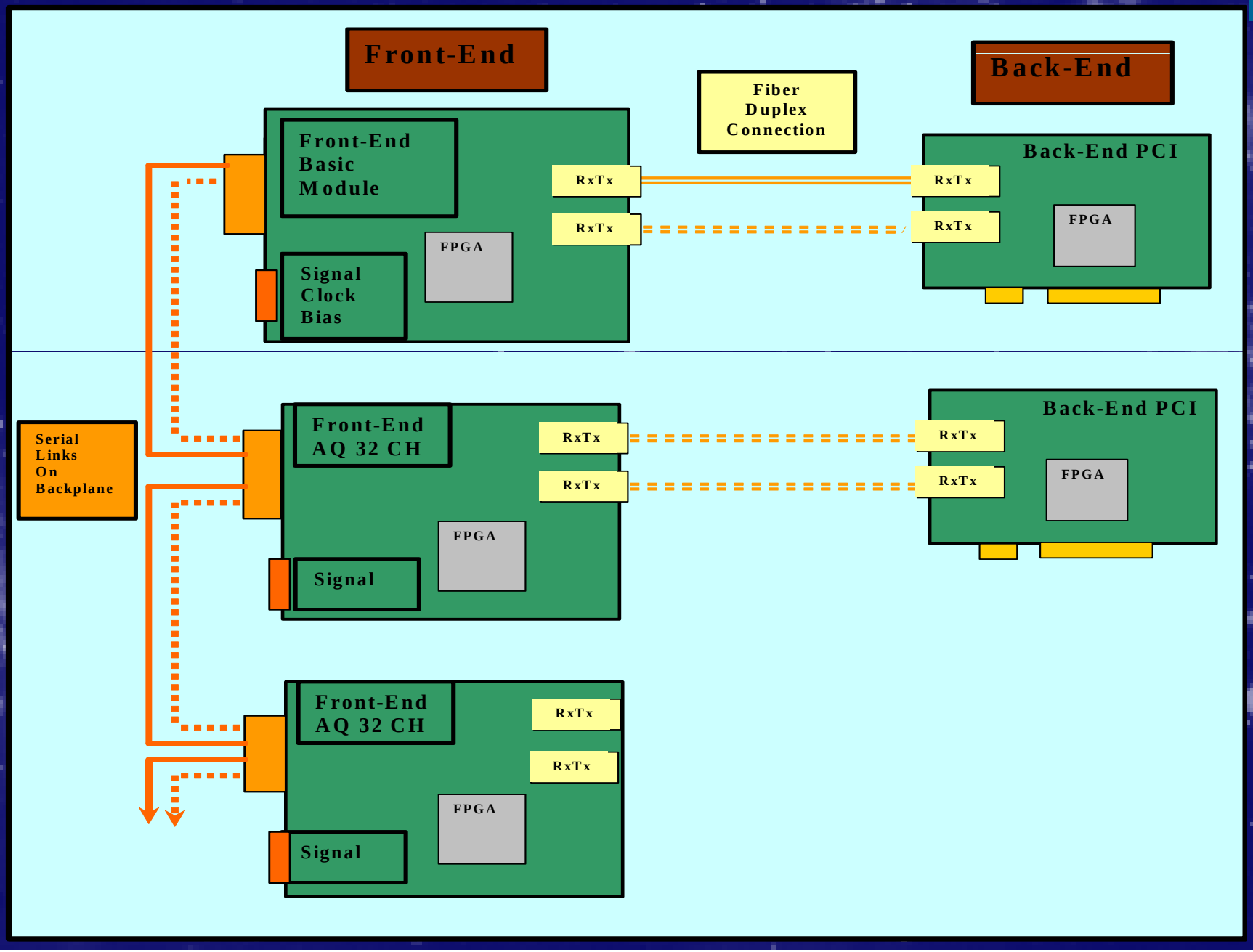
Read-out of Multi-channel Detectors like Hawaii II RG with AQ 32 Board and Basic Board



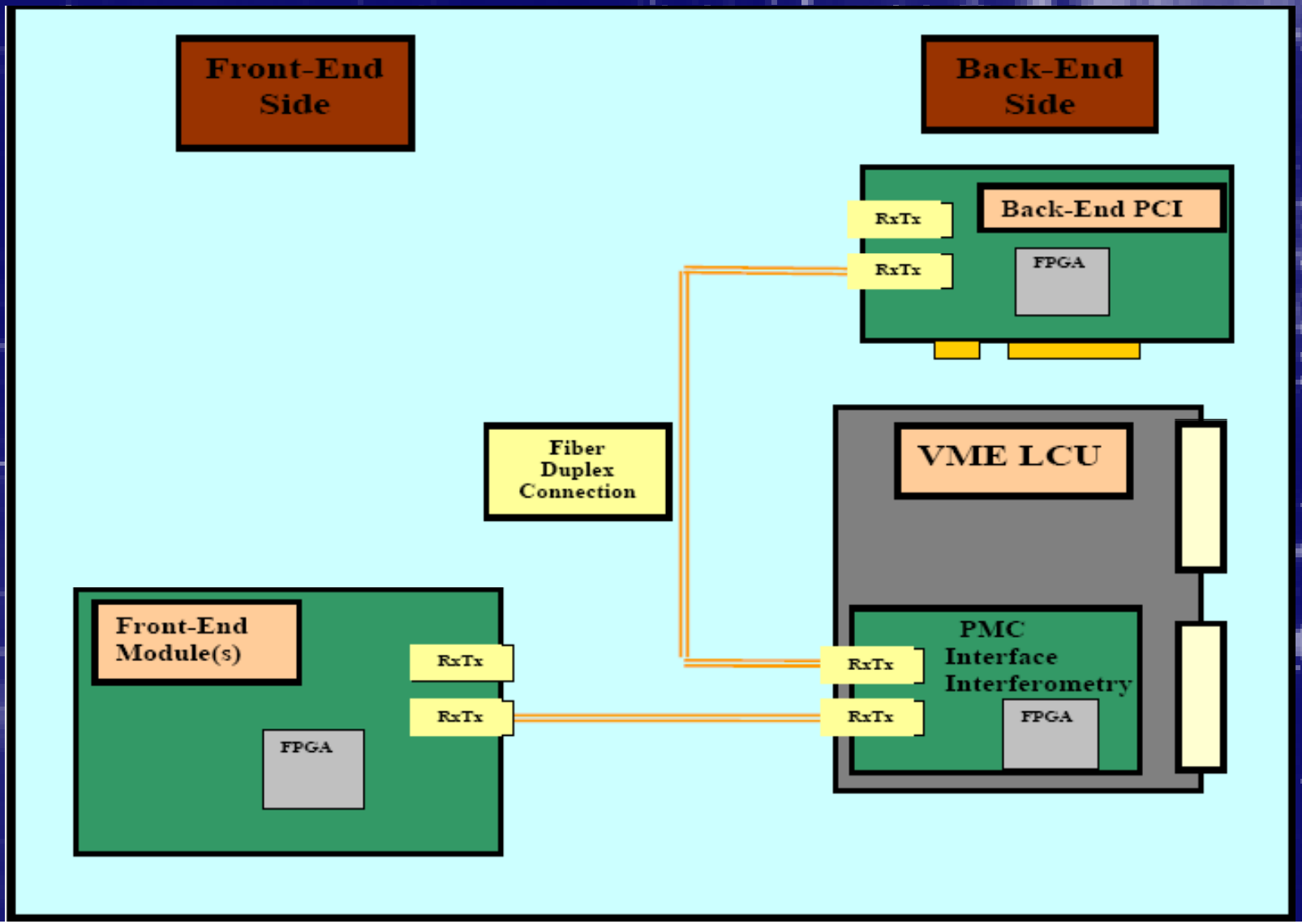
More Bandwidth and Different Routing

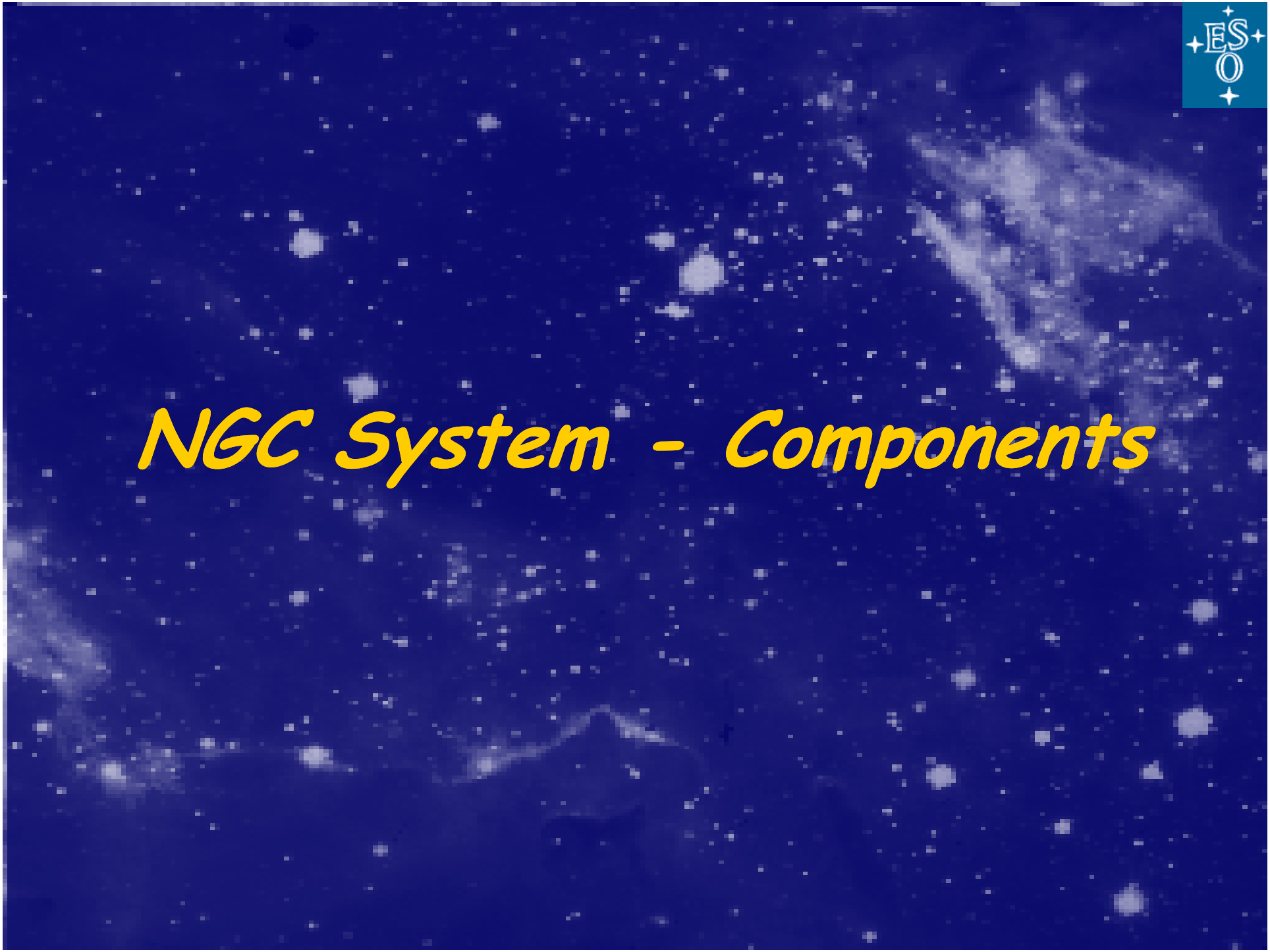


64 and more Video Channels



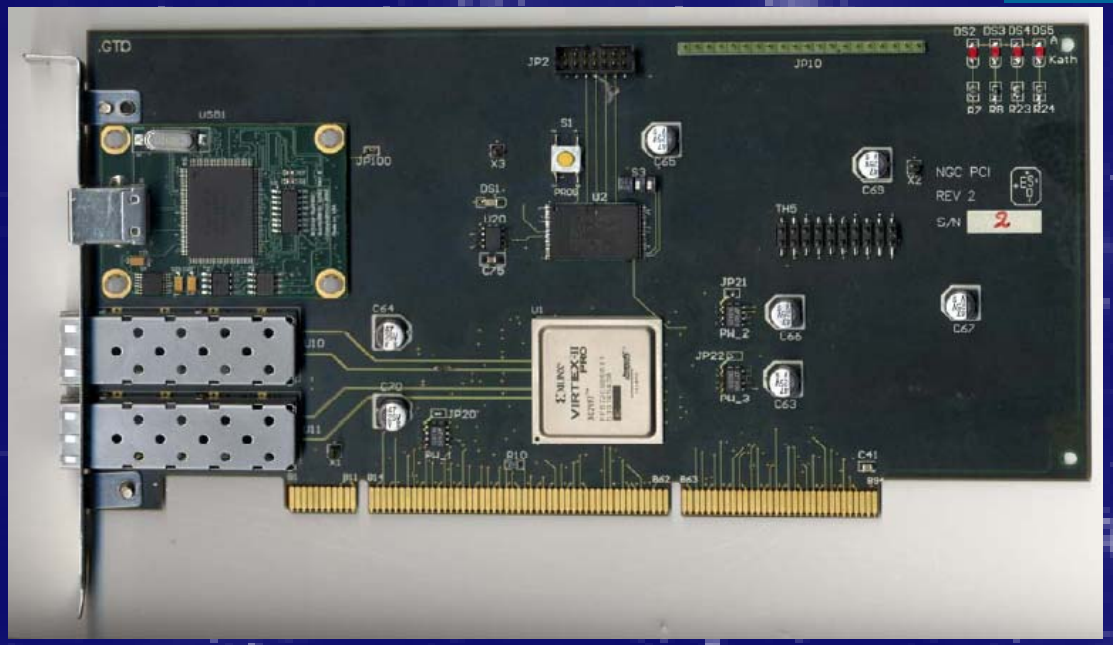
Real Time VLTI INTERFACE : PMC Based Low Latency DMA Channel




NGC System - Components

PCI Back-End

- Direct interface from FPGA to PCI without glue logic
- PCI master and PCI slave are independent
- Scatter – Gather DMA
- Communication and data transfers all on serial link
- Handshake communication to Front-End
- Serial link data rate between front and back-end ~ 200MByte/s
- PCI Interface 64 Bit/33MHz



VirtexII Pro

Contains :

PCI 64 IF (IP)

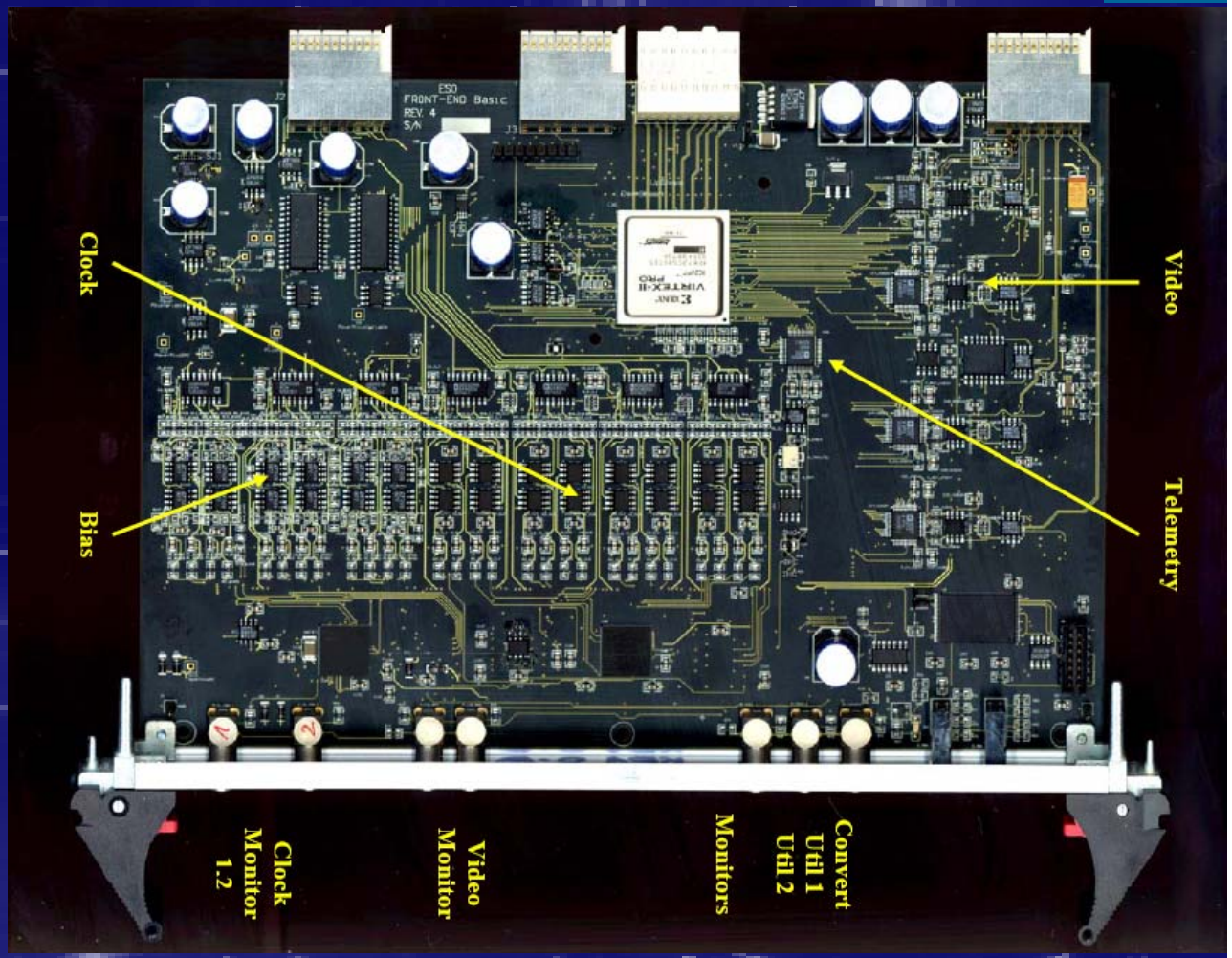
Communication

DMA Data Transfer

Rocket I/O Transceivers

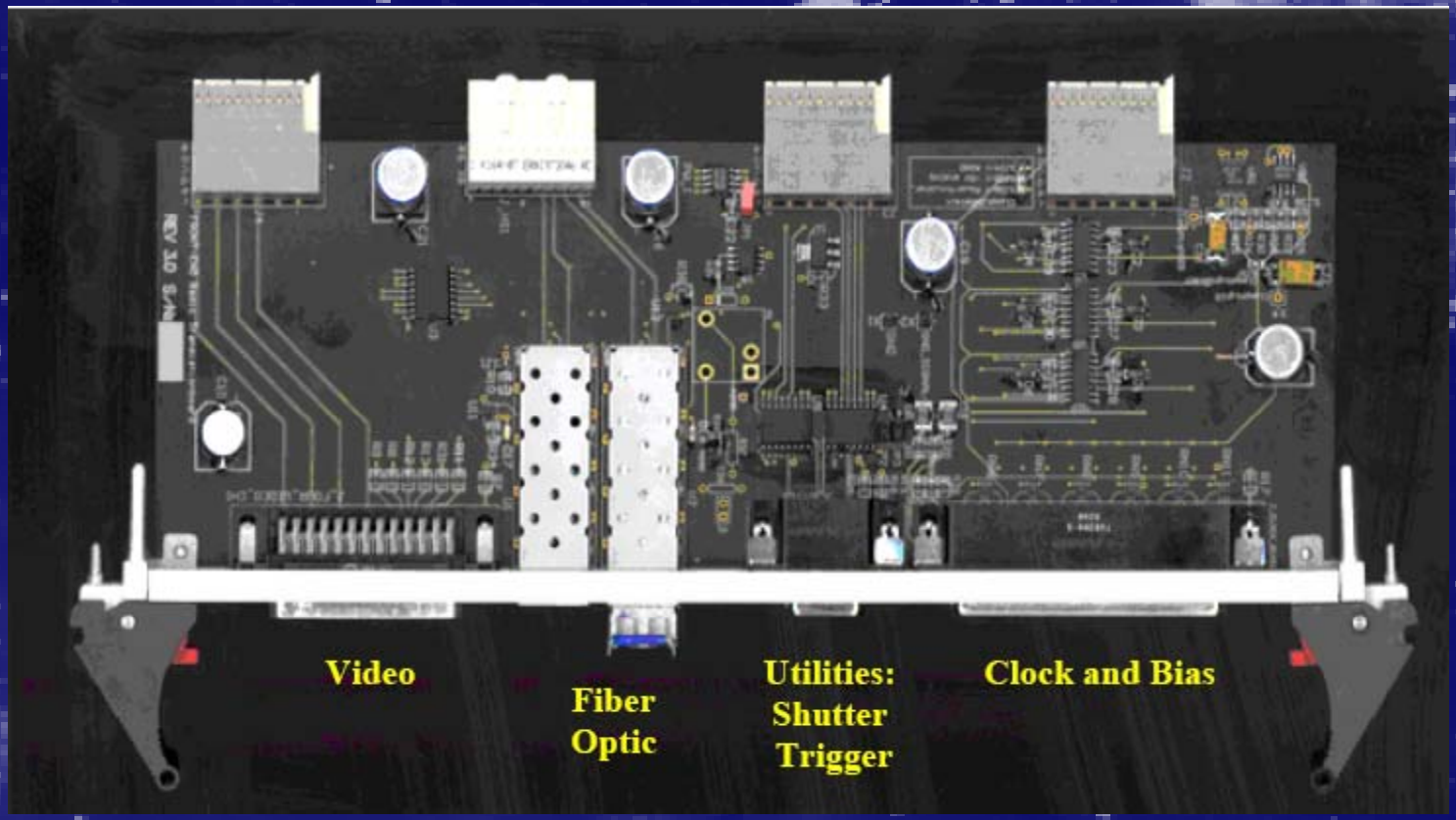
Basic Board

- Four Video channels
- 18 clocks, 20 biases
- Telemetry
- Monitoring
- Integrated shutter Control
- Galvanic isolated trigger input and control outputs (on Transition board)



FPGA contains link interface for communication and data transfer with RocketIO transceivers, system administration, sequencer, interface to Adc's clock and bias, telemetry and monitoring

Transition Board Front-End



AQ32 Board

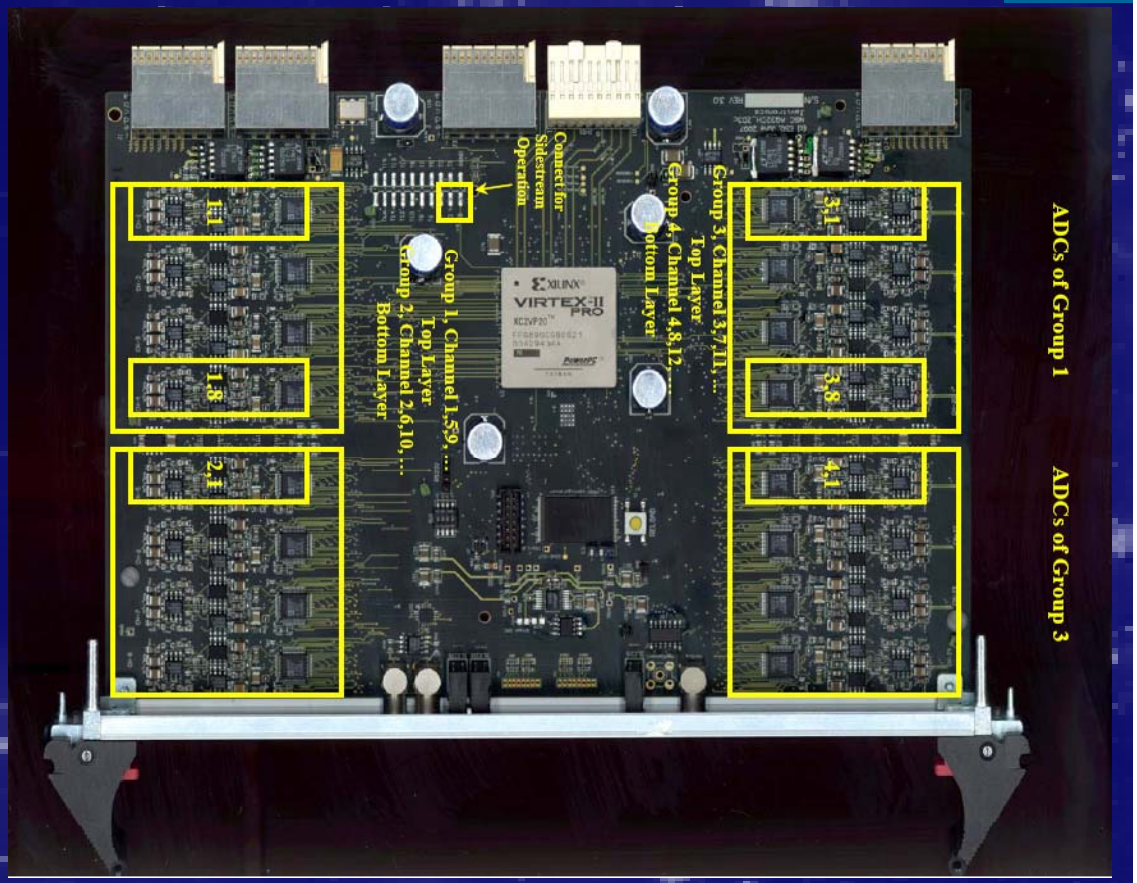
AQ32 is a VME size board

No glue logic to module Functions – all done in FPGA.

32 ADC channels

Serial Link data rate ~ 200MByte/s

Handshaked communication to back-end



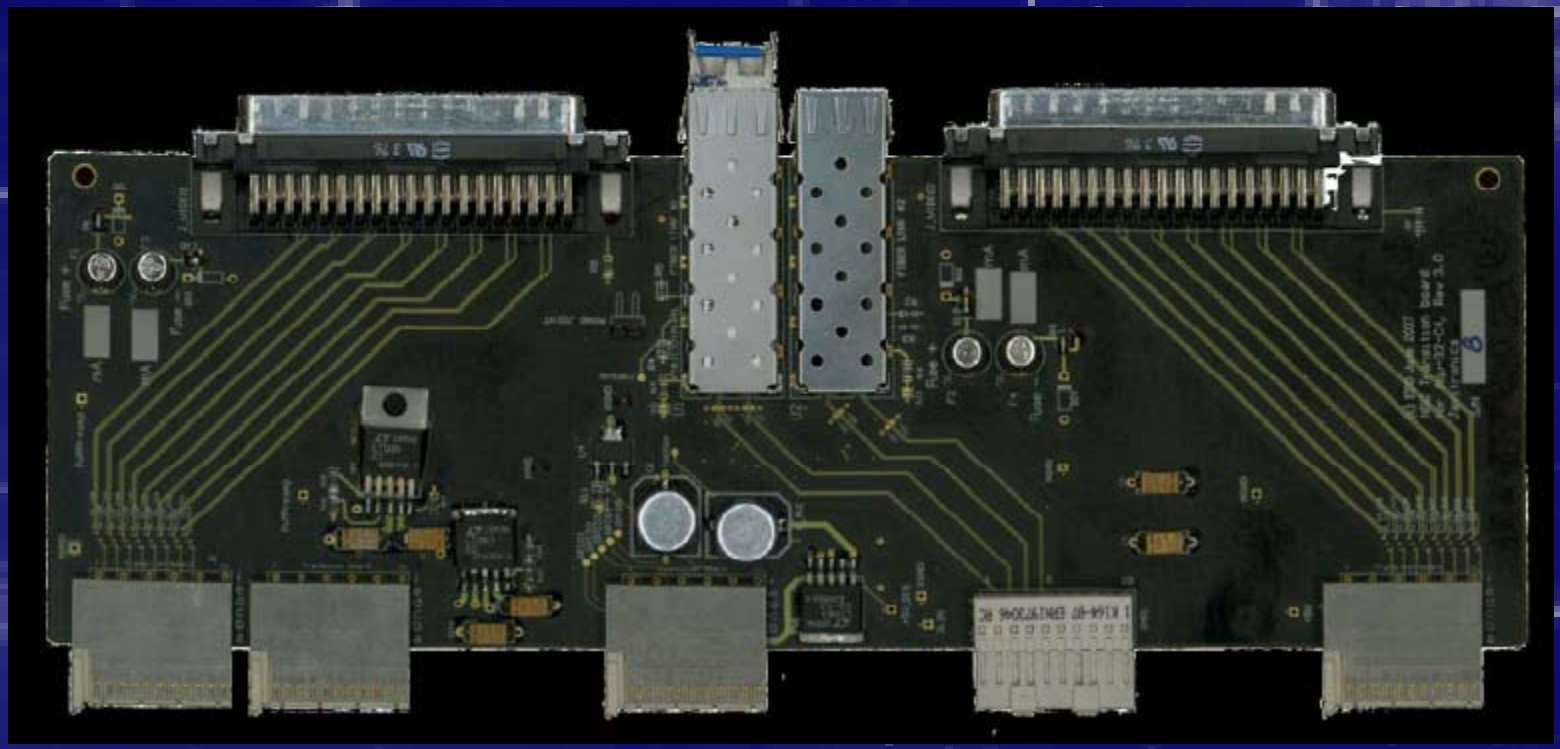
FPGA contains link interface for communication and data transfer with RocketIO transceivers, system administration, interface to acquisition, monitoring

Transition Board AQ32

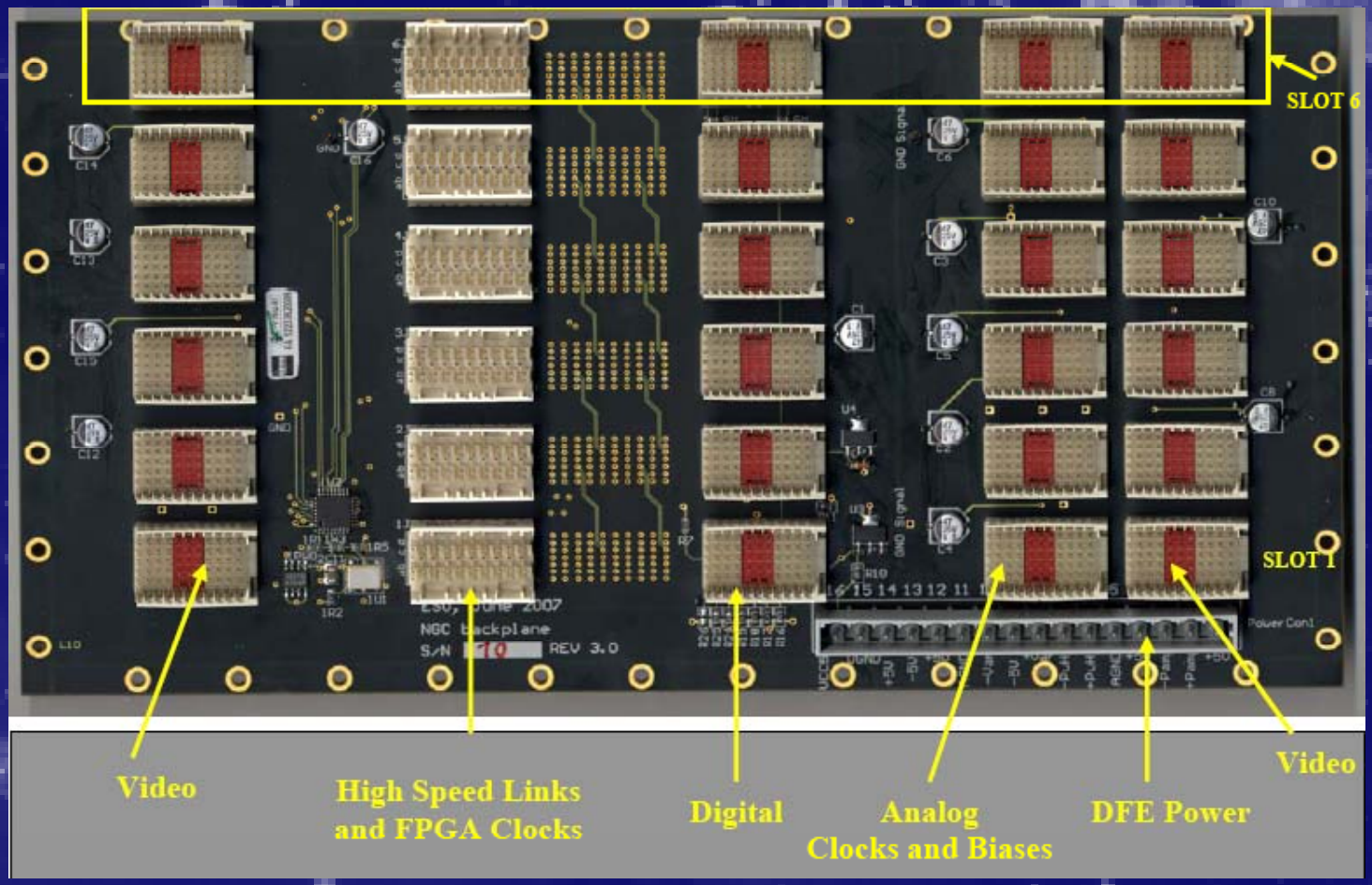
Video Input Channel 1 - 16

Fiber optics Transceivers

Video Input Channel 17 - 32



NGC Backplane



Real Time VLTI INTERFACE :
PMC Board
(installed in PMC slot of MVME6100)

Documents

Next Generation detector Controller Requirements
ESO-Doc. No. VLT-SPE-ESO-13660-3207 by *D. Baade* (Mar/11/2004)

NGC USER MANUAL
Doc.-No. VLT-MAN-ESO-13660-4510

Interface Control Document for the New General Detector Controller (NGC)
ESO-Doc. No. VLT-ICD-ESO-13660-4009 by *M. Meyer et al.* (Feb/20/2007)

Papers

NGC Front-End for CCDs and AO Applications
Paper for SDW 2005 in Taormina (Italy) by *J. Reyes et al.* (Jun/24/2005)

NGC - Detector Array Controller based on High Speed Serial Link Technology
Paper for SDW 2005 in Taormina (Italy) by *M. Meyer et al.* (Jun/24/2005)

Presentations

ESODAC - Study for a new ESO Detector Array Controller
Presentation at ESO by *M. Meyer* (Oct/24/2003)

Study on the hardware of the ESO Next Generation Detector Controller (ENGDC)
Presentation at ESO by *J. Reyes* (Nov/07/2003)

Prototyping NGC
Presentation at ESO by *M. Meyer* (Mar/19/2004)

NGC progress, common platform and deliverables
Presentation at ESO by *J. Reyes* (Mar/19/2004)

CCD head for AO
Presentation at ESO by *J. Reyes* (Dec/08/2004)

NGC - Detector Array Controller based on High Speed Serial Link Technology
Presentation of NGC "first light" with PICNIC array by *M. Meyer* (Dec/05/2005)

NGC and L3 CCDs
Presentation of NGC "first light" with L3 CCDs by *M. Meyer* (Dec/05/2005)

http://www.eso.org/projects/ngc/