

MAIT

What does it mean ?

- Major Area Integration Team ?
- Multidisciplinary Accident Investigation Team ?
- McCabe's Artificially Intelligence Tipper ?
(www.mymait.com)
- Maintenance Assistance and Instruction Team ?
- Martial Art Instructor / Trainer ?

.... **best guess :**

- **Manufacturing, Assembly, Integration and Testing !**

OK, acronym problem solved. Let's build an NGC ...

... starting with the Manufacturing / Assembly !

Procurement

BOM (Bill of Materials)

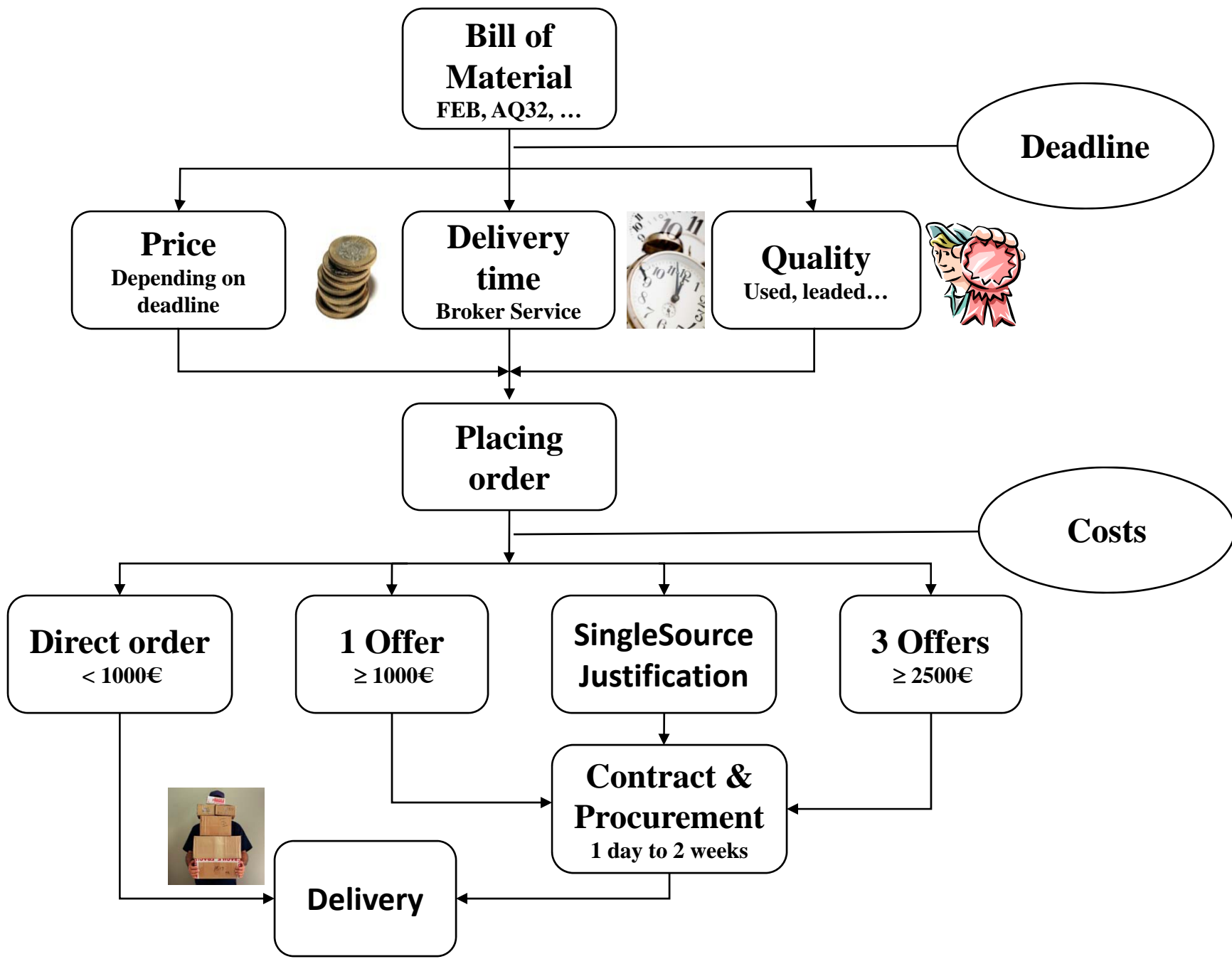
BOM from design file

Designator		Comment	Footprint
C1_BIAS1		100nF	CC2013-0805
C1_BIAS2		100nF	CC2013-0805
C1_BIAS3		100nF	CC2013-0805
C100_VIDEO1		10uF/25V	CC4532-1812
C100_VIDEO2		10uF/25V	CC4532-1812
C100_VIDEO3		10uF/25V	CC4532-1812
C100_VIDEO4		10uF/25V	CC4532-1812
PW_3		LT1963AES8-1.5V	SO-G8

BOM after inspection

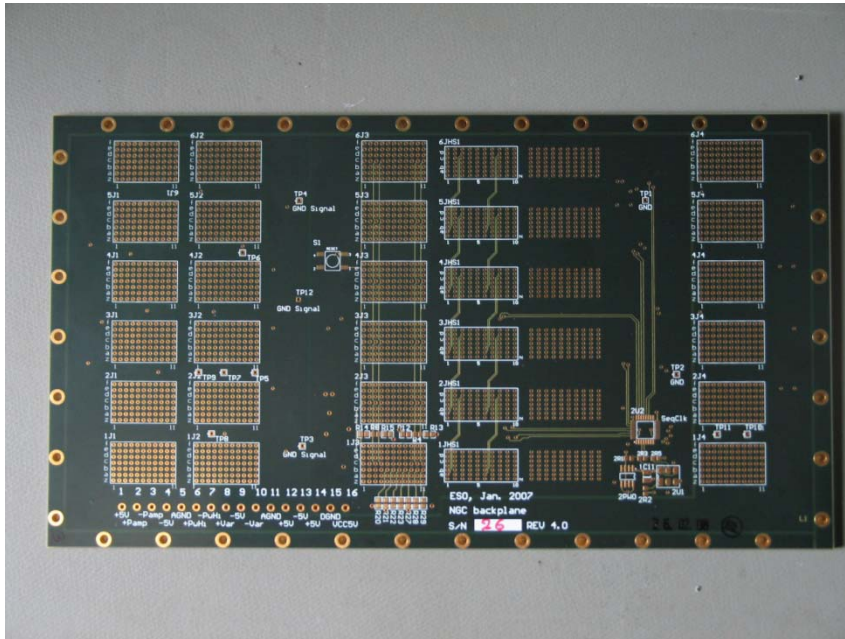
Designator	Article No.	Comment	Footprint
C1_BIAS1	A03600	KerKo 100nF ±10% 50V X7R	SMD-0805
C1_BIAS2	A03600	KerKo 100nF ±10% 50V X7R	SMD-0805
C1_BIAS3	A03600	KerKo 100nF ±10% 50V X7R	SMD-0805
C100_VIDEO1	A08085	KerKo 10uF ±10% 25V X7R	SMD-1812
C100_VIDEO2	A08085	KerKo 10uF ±10% 25V X7R	SMD-1812
C100_VIDEO3	A08085	KerKo 10uF ±10% 25V X7R	SMD-1812
C100_VIDEO4	A08085	KerKo 10uF ±10% 25V X7R	SMD-1812
PW_3	2430	LT1963AES8-1.5#PBF	8-SOIC N 1,27mm Pitch

BOM of FEB contains 930 parts

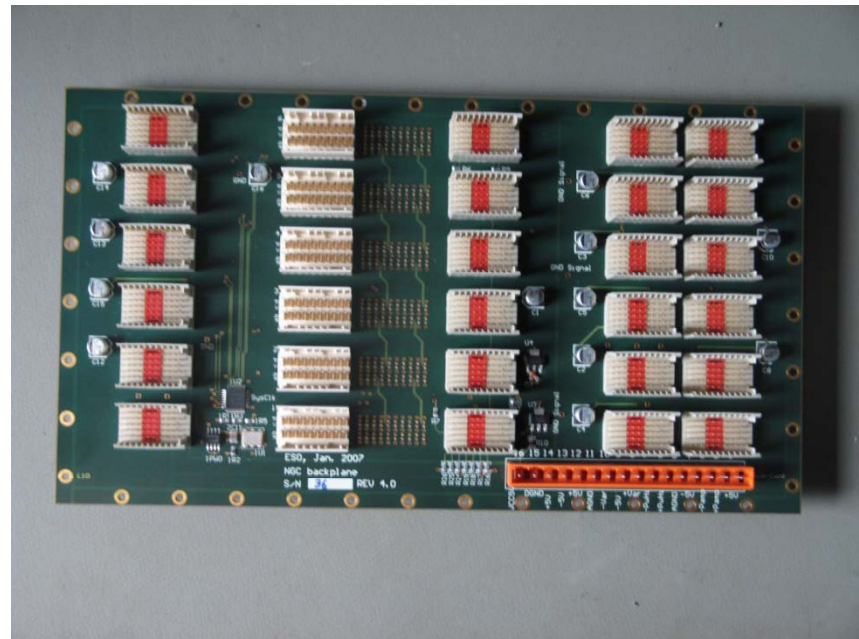


Population Assembly

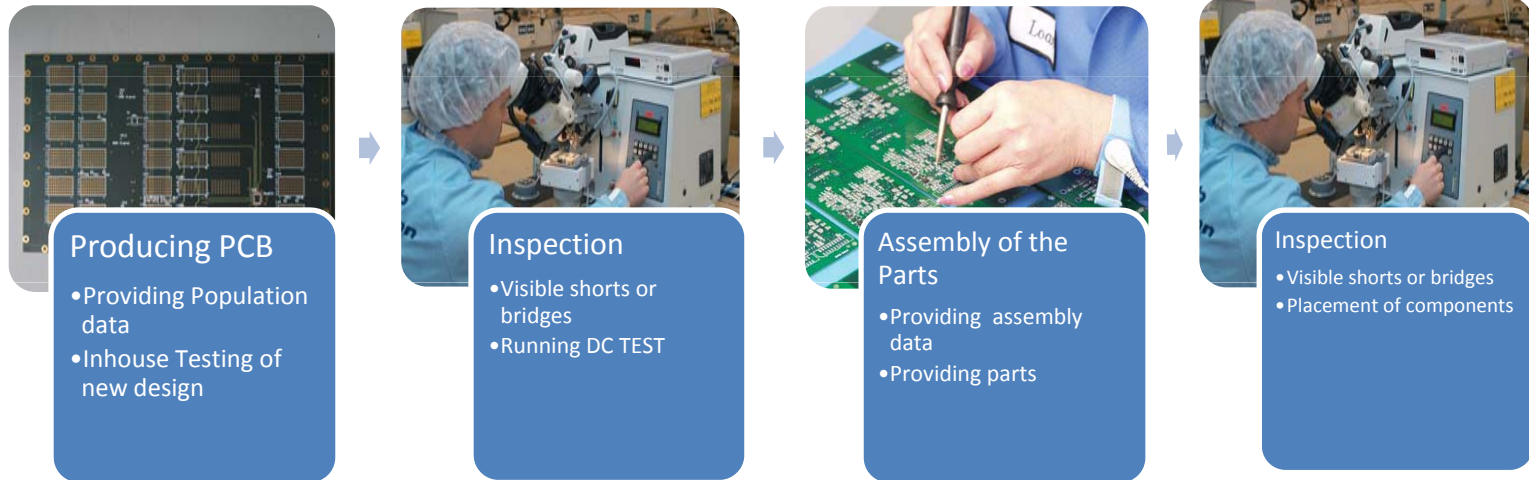
Unpopulated PCB



Populated PCB



Population Assembly



Population Assembly



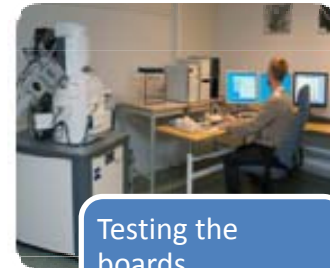
Assembly of the connectors

- Providing assembly data
- Providing connectprs



Inspection

- Placement of the connectors
- Straight pins etc.



Testing the boards

- DC Test
- Running application



Next we need to take a look at the TWIKI pages....

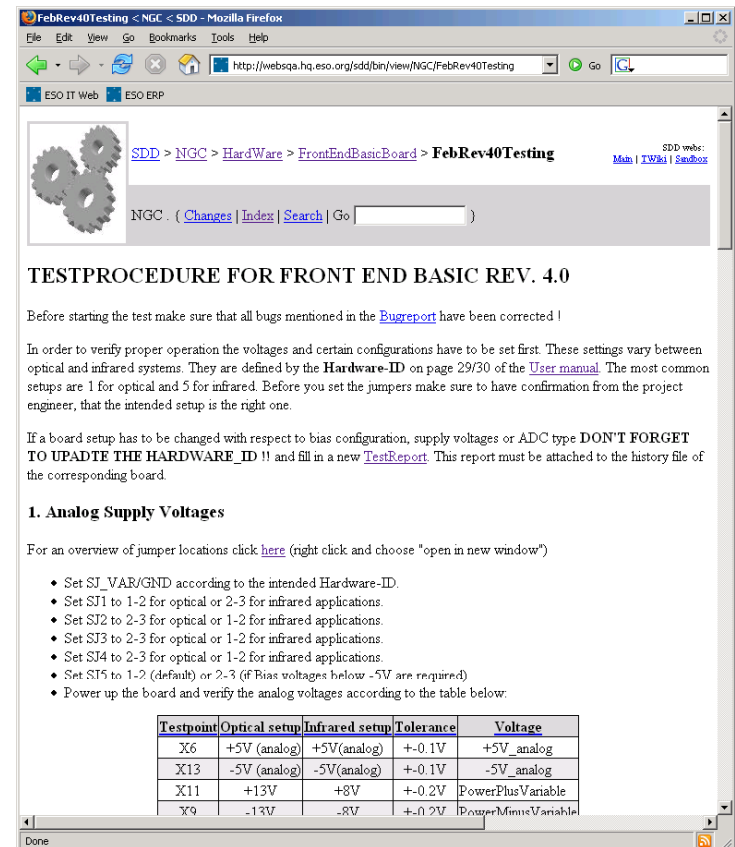
TWIKI contains everything we need

BIGGEST ADVANTAGES:

- HTML based, therefore platform and OS independent. Only browser required.
- No excuse not to use it.
- Accessible from both sides of the Atlantic.
- All NGC related documents are in one place.
- Possibility of creating links instead of keeping redundant information in different places.

Testing step 1: Test procedure

- Detailed test procedures for each board are available from TWIKI.
- Designers are not the only ones who can test a board. Also less experienced personnel is enabled to do testing, thus minimizing the risk of single point failures.
- Instructions how to configure/reconfigure a board for an optical or an infrared system (if applicable) - making it an LRU.



The screenshot shows a Mozilla Firefox browser window displaying the TWIKI page for 'FebRev40Testing'. The browser's address bar shows the URL: <http://websqa.hq.eso.org/sdd/bin/view/NGC/FebRev40Testing>. The page content includes a breadcrumb trail: SDD > NGC > Hardware > FrontEndBasicBoard > FebRev40Testing. Below the breadcrumb is a search bar with the text 'NGC : (Changes | Index | Search | Go [])'. The main heading is 'TESTPROCEDURE FOR FRONT END BASIC REV. 4.0'. The text below the heading provides instructions for testing, including a warning to check for bugs in the Bugreport and a note to update the Hardware-ID. A section titled '1. Analog Supply Voltages' lists several steps for setting up the board. At the bottom of the page, there is a table with the following data:

Testpoint	Optical setup	Infrared setup	Tolerance	Voltage
X6	+5V (analog)	+5V(analog)	+0.1V	+5V_analog
X13	-5V (analog)	-5V(analog)	+0.1V	-5V_analog
X11	+13V	+8V	+0.2V	PowerPlusVariable
X9	-13V	-8V	+0.2V	PowerMinusVariable

Testing step 2: Board Test tools

- A total of 18 clocks and 20 biases have to be tested over the complete output range.
- Manual test would take several hours.
- Linux test script automates this test cutting down test time to 10-15 minutes without the need for user intervention.
- No additional software is required. Linux has everything you need.



```
xterm
odt7 ngcmgr:~/scripts 1012 >
odt7 ngcmgr:~/scripts 1012 > ./ngcDcsTestCris.sh -bias
Start server ...
Warning: ccsInit failed
Checking board id ...
Loading voltage table cldcTest.v ...
Setting DAC offset for BIAS test ...
*****
* TESTING BIAS 1..16 *
*****
Testing DC1 with 0.3V - Min:.15V Max:.45V Tel:0.274V - Diff:-.026V (Chan:36) -> OK.
Testing DC2 with 0.3V - Min:.15V Max:.45V Tel:0.412V - Diff:.112V (Chan:37) -> OK.
Testing DC3 with 0.3V - Min:.15V Max:.45V Tel:0.383V - Diff:.083V (Chan:38) -> OK.
Testing DC4 with 0.3V - Min:.15V Max:.45V Tel:0.306V - Diff:.006V (Chan:39) -> OK.
Testing DC5 with 0.3V - Min:.15V Max:.45V Tel:0.358V - Diff:.058V (Chan:40) -> OK.
Testing DC6 with 0.3V - Min:.15V Max:.45V Tel:0.395V - Diff:.095V (Chan:41) -> OK.
Testing DC7 with 0.3V - Min:.15V Max:.45V Tel:0.405V - Diff:.105V (Chan:42) -> OK.
Testing DC8 with 0.3V - Min:.15V Max:.45V Tel:0.394V - Diff:.094V (Chan:43) -> OK.
Testing DC9 with 0.3V - Min:.15V Max:.45V Tel:0.318V - Diff:.018V (Chan:44) -> OK.
Testing DC10 with 0.3V - Min:.15V Max:.45V Tel:0.405V - Diff:.105V (Chan:45) -> OK.
Testing DC11 with 0.3V - Min:.15V Max:.45V Tel:0.317V - Diff:.017V (Chan:46) -> OK.
Testing DC12 with 0.3V - Min:.15V Max:.45V Tel:0.387V - Diff:.087V (Chan:47) -> OK.
Testing DC13 with 0.3V - Min:.15V Max:.45V Tel:0.317V - Diff:.017V (Chan:48) -> OK.
Testing DC14 with 0.3V - Min:.15V Max:.45V Tel:0.336V - Diff:.036V (Chan:49) -> OK.
Testing DC15 with 0.3V - Min:.15V Max:.45V Tel:0.369V - Diff:.069V (Chan:50) -> OK.
Testing DC16 with 0.3V - Min:.15V Max:.45V Tel:0.237V - Diff:-.063V (Chan:51) -> OK.
Testing DC1 with .6V - Min:.45V Max:.75V Tel:0.574V - Diff:-.026V (Chan:36) -> OK.
Testing DC2 with .6V - Min:.45V Max:.75V Tel:0.714V - Diff:.114V (Chan:37) -> OK.
Testing DC3 with .6V - Min:.45V Max:.75V Tel:0.676V - Diff:.076V (Chan:38) -> OK.
Testing DC4 with .6V - Min:.45V Max:.75V Tel:0.607V - Diff:.007V (Chan:39) -> OK.
Testing DC5 with .6V - Min:.45V Max:.75V Tel:0.655V - Diff:.055V (Chan:40) -> OK.
Testing DC6 with .6V - Min:.45V Max:.75V Tel:0.692V - Diff:.092V (Chan:41) -> OK.
Testing DC7 with .6V - Min:.45V Max:.75V Tel:0.705V - Diff:.105V (Chan:42) -> OK.
Testing DC8 with .6V - Min:.45V Max:.75V Tel:0.694V - Diff:.094V (Chan:43) -> OK.
Testing DC9 with .6V - Min:.45V Max:.75V Tel:0.615V - Diff:-.015V (Chan:44) -> OK.
```

```
xterm
*****
TestReport for FEB with hardware ID 1
Errors are listed below:
-----
CLKL03 is .161V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.739V Telchan: 4)
CLKL04 is .151V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.749V Telchan: 6)
CLKL06 is .155V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.745V Telchan: 10)
CLKL011 is .169V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.731V Telchan: 20)
CLKL013 is .166V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.734V Telchan: 24)
CLKL015 is .172V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.728V Telchan: 28)
CLKL03 is .153V outside setpoint (Set: -9.6V Min:-9.75V Max:-9.45V Tel: -9.447V Telchan: 4)
CLKL011 is .154V outside setpoint (Set: -9.6V Min:-9.75V Max:-9.45V Tel: -9.446V Telchan: 20)
CLKL013 is .154V outside setpoint (Set: -9.6V Min:-9.75V Max:-9.45V Tel: -9.446V Telchan: 24)
CLKL015 is .161V outside setpoint (Set: -9.6V Min:-9.75V Max:-9.45V Tel: -9.439V Telchan: 28)
CLKL03 is .151V outside setpoint (Set: -9.3V Min:-9.45V Max:-9.15V Tel: -9.149V Telchan: 4)
CLKL011 is .151V outside setpoint (Set: -9.3V Min:-9.45V Max:-9.15V Tel: -9.149V Telchan: 20)
CLKL013 is .154V outside setpoint (Set: -9.3V Min:-9.45V Max:-9.15V Tel: -9.146V Telchan: 24)
CLKL015 is .158V outside setpoint (Set: -9.3V Min:-9.45V Max:-9.15V Tel: -9.142V Telchan: 28)
CLKL03 is .151V outside setpoint (Set: -9.0V Min:-9.15V Max:-8.85V Tel: -8.849V Telchan: 4)
CLKL015 is .157V outside setpoint (Set: -9.0V Min:-9.15V Max:-8.85V Tel: -8.843V Telchan: 28)
CLKL015 is .156V outside setpoint (Set: -8.7V Min:-8.85V Max:-8.55V Tel: -8.544V Telchan: 28)
CLKL015 is .156V outside setpoint (Set: -8.4V Min:-8.55V Max:-8.25V Tel: -8.244V Telchan: 28)
CLKL015 is .154V outside setpoint (Set: -8.1V Min:-8.25V Max:-7.95V Tel: -7.946V Telchan: 28)
CLKL015 is .154V outside setpoint (Set: -7.8V Min:-7.95V Max:-7.65V Tel: -7.646V Telchan: 28)
CLKL015 is .152V outside setpoint (Set: -7.5V Min:-7.65V Max:-7.35V Tel: -7.348V Telchan: 28)
CLKHI8 is .155V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.745V Telchan: 15)
CLKHI12 is .179V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.721V Telchan: 23)
CLKHI14 is .152V outside setpoint (Set: -9.9V Min:-10.05V Max:-9.75V Tel: -9.748V Telchan: 27)
CLKHI12 is .158V outside setpoint (Set: -9.6V Min:-9.75V Max:-9.45V Tel: -9.442V Telchan: 23)
CLKHI12 is .152V outside setpoint (Set: -9.3V Min:-9.45V Max:-9.15V Tel: -9.148V Telchan: 23)

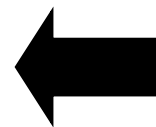
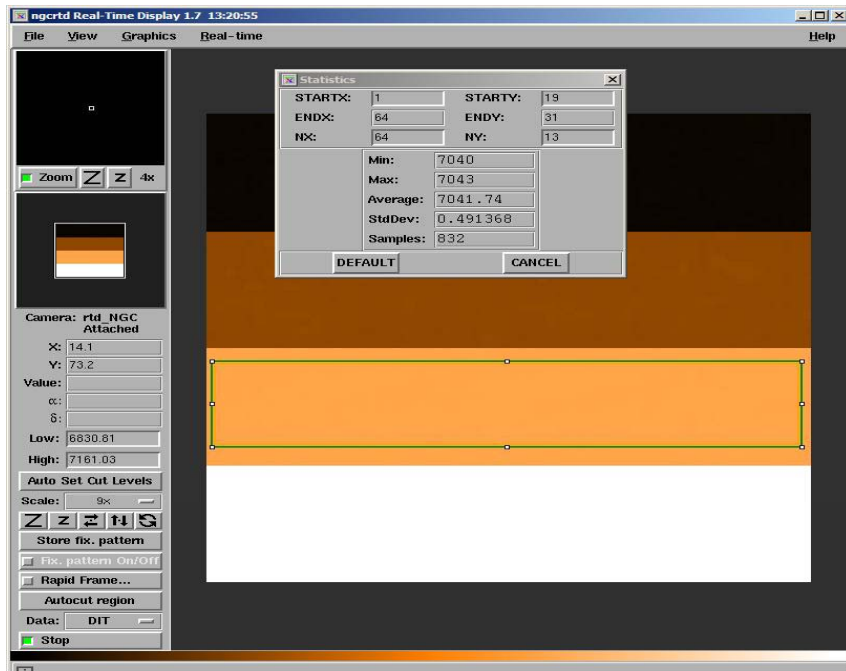
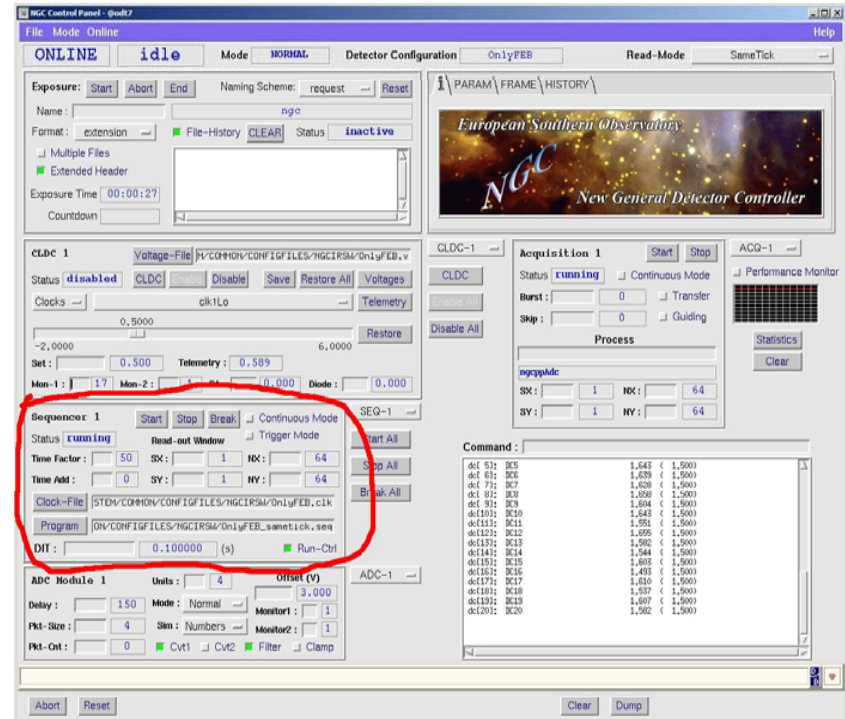
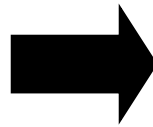
==> ngcDcsTestCris.sh successfully completed
odt7 ngcmgr:~/scripts 1015 >
```



- Errors encountered during test are logged to file for later analysis.

Testing step 2: Board Test tools (cont.)

- End to end noise test for clock/bias and video using the NGC sequencer.
- Requires only a cable between clock/bias connector and video input.



- Any noise problem in either clock/bias or video chain will show up in the RTD.

Testing step 3: Test report

- Test report to be filled out after successful configuration and test of each board.
- Contains detailed information about the configuration of each board (voltages, Bias setup, ADC configuration, Firmware, Hardware-ID etc.)
- Double check of all voltages and settings against the numbers given in the TWIKI test procedure and User manual



Test Report for NGC Front End Basic Rev. 4.0

Use the *File > SavePage as* Command to download a local copy. After successful testing this report must be appended to the history file of the board.

Tested by: Date:

Board number: Firmware version: Hardware ID:

1. Analog Supply Voltages: (Tolerance $\pm 0.2V$, Ripple: max.20mV_{pp})

PowerPlusHigh (V)	<input type="text" value="28.5"/>	Ripple (mV _{pp})	<input type="text" value="15"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
PowerMinusHigh (V)	<input type="text" value="-12.8"/>	Ripple (mV _{pp})	<input type="text" value="10"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
PowerPlusVariable (V)	<input type="text" value="13.2"/>	Ripple (mV _{pp})	<input type="text" value="14"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
PowerMinusVariable (V)	<input type="text" value="-12.9"/>	Ripple (mV _{pp})	<input type="text" value="12"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
PowerMinusDAC (V)	<input type="text" value="-12.8"/>	Ripple (mV _{pp})	<input type="text" value="8"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
-5V Analog (V)	<input type="text" value="-5.0"/>	Ripple (mV _{pp})	<input type="text" value="10"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
+5V Analog (V)	<input type="text" value="5.1"/>	Ripple (mV _{pp})	<input type="text" value="12"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
+2.5V_Power (V)	<input type="text" value="2.5"/>	Ripple (mV _{pp})	<input type="text" value="6"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED

* NOTE: Voltage depends on Hardware-ID. See user manual and Twiki Testreport for details.

Voltages match Hardware-ID in User Manual? Yes NO

2. Digital Supply Voltages: (Tolerance $\pm 0.1V$, Ripple: max.20mV_{pp})

3.3V Digital (V)	<input type="text" value="3.3"/>	Ripple (mV _{pp})	<input type="text" value="15"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
2.5V Digital JP3 (V)	<input type="text" value="2.5"/>	Ripple (mV _{pp})	<input type="text" value="10"/>	<input type="radio"/> PASSED <input type="radio"/> FAILED
2.5V Digital JP4 (V)	<input type="text" value="2.4"/>	Ripple (mV _{pp})	<input type="text" value="12"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED
1.5V Digital JP5 (V)	<input type="text" value="1.5"/>	Ripple (mV _{pp})	<input type="text" value="10"/>	<input checked="" type="radio"/> PASSED <input type="radio"/> FAILED

- To be attached to the history file of each board.



FEB_Revision_4 < NGC < SDD - Mozilla Firefox

http://websqa.hq.eso.org/sdd/bin/vix

ESO IT Web ESO ERP

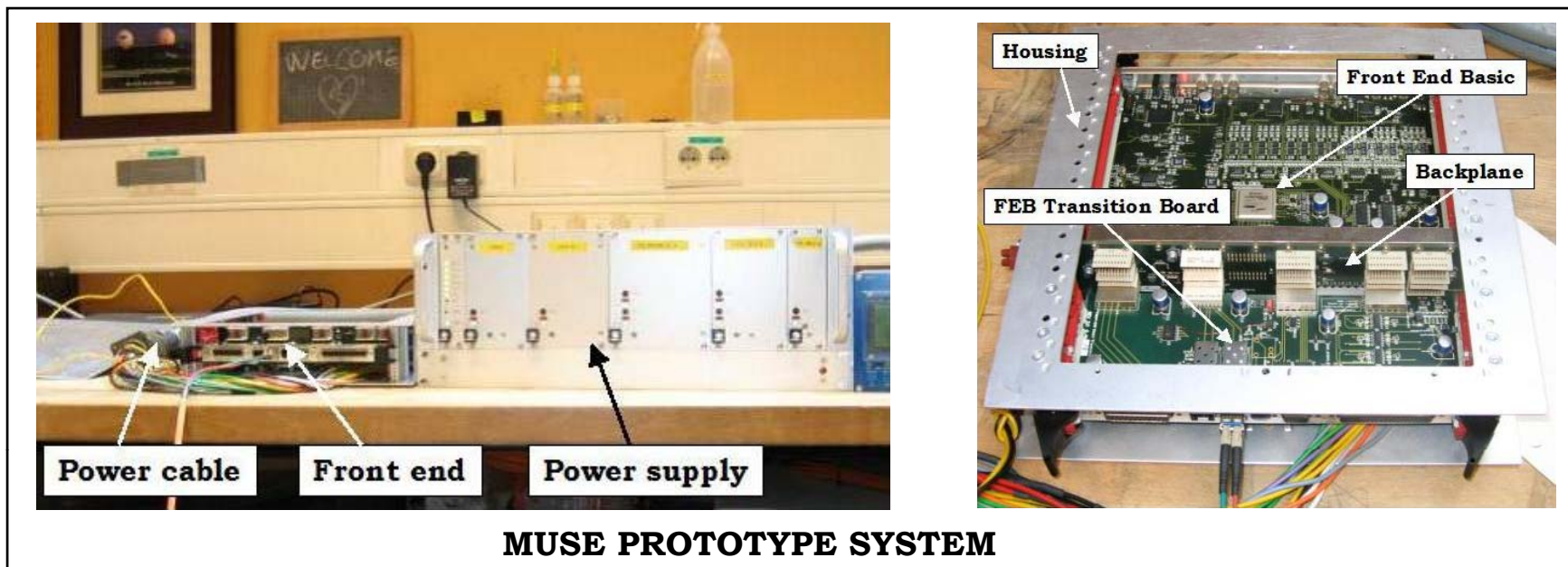
SDD > NGC > HardWare > FrontEndBasicBoard >
 History FEB > **FEB_Revision_4**

NGC . ([Changes](#) | [Index](#) | [Search](#) | Go)

Serial number	revision	used by	project	*_Firmware Version
6	revision 4	Christoph	Voltage regulator Test	
7	revision 4	Stefan	Reference PCB (empty)	
8	revision 4	Christoph	first populated test board	
9	revision 4	Manfred	system testing	
10	revision 4	Javier	CCD Test	
11	revision 4	On stock	to be tested	
12	revision 4	Leander	KMOS	
13	revision 4	Lab 071	MUSE prototype	4.1.5
14	revision 4	Lab 071	ZIMPOL (to be tested)	4.1.5
15	revision 4	Leander	system test	
16	revision 4	Lab 071	to be fixed	4.1.5
17	revision 4	Lab 071	to be fixed	

-- ChristophGeimer - 17 Oct 2007 -- ManfredMeyer - 19 Jan 2008

Integration

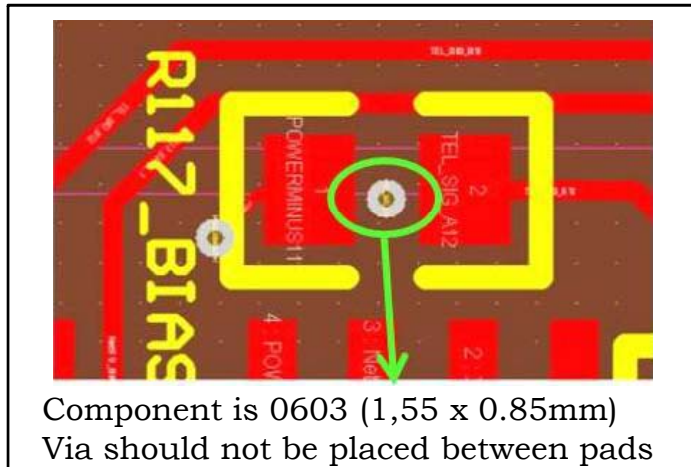


Goals:

- Make sure that all individually tested boards work properly together in the final system.
- Fine-tuning of voltages in the final setup taking into account number of boards and final cable length.
- Verification of clock/bias and video chain. Using the available test tools this test can be done in ~ 30 - 45min.
- TO DO: Create integration test report listing the most important system parameters. To be included in the project's TWIKI page.

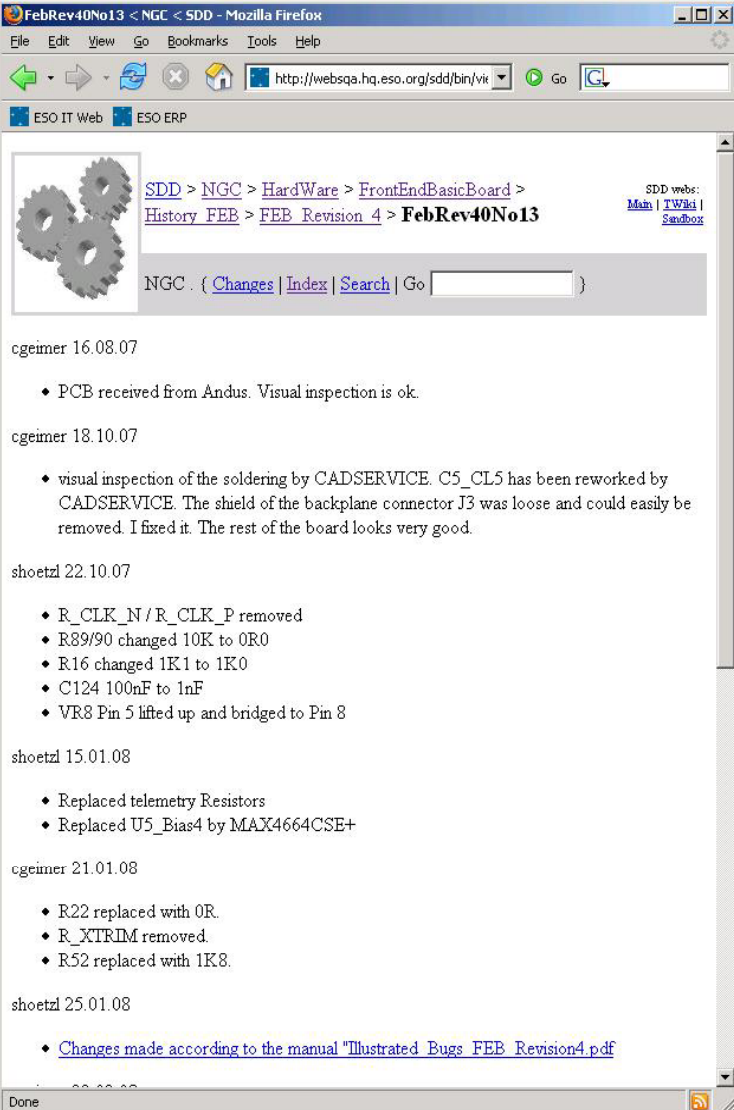
Maintenance

- Basic procedure can be found in the NGC production manual.
- All changes made to a board must be documented in the history file.
- The TWIKI bug report provides useful feedback to designers in order to avoid Problems in new revisions.



TO DO:

- Compile a “most common failures” –list for each board based on experience gained during maintenance.
- Prepare list for “preventive maintenance”



The screenshot shows a web browser window displaying a board history file for "FebRev40No13". The browser address bar shows the URL "http://websqa.hq.eso.org/sdd/bin/vik". The page content includes a navigation menu with links for "SDD > NGC > HardWare > FrontEndBasicBoard > History FEB > FEB Revision 4 > FebRev40No13". Below the navigation menu, there is a search bar and a list of changes made to the board. The changes are listed with dates and descriptions:

- cgeimer 16.08.07
 - PCB received from Andus. Visual inspection is ok.
- cgeimer 18.10.07
 - visual inspection of the soldering by CADSERVICE. C5_CL5 has been reworked by CADSERVICE. The shield of the backplane connector J3 was loose and could easily be removed. I fixed it. The rest of the board looks very good.
- shoetzi 22.10.07
 - R_CLK_N/R_CLK_P removed
 - R89/90 changed 10K to 0R0
 - R16 changed 1K1 to 1K0
 - C124 100nF to 1nF
 - VR8 Pin 5 lifted up and bridged to Pin 8
- shoetzi 15.01.08
 - Replaced telemetry Resistors
 - Replaced U5_Bias4 by MAX4664CSE+
- cgeimer 21.01.08
 - R22 replaced with 0R.
 - R_XTRIM removed.
 - R52 replaced with 1K8.
- shoetzi 25.01.08
 - [Changes made according to the manual "Illustrated_Bugs_FEB_Revision4.pdf"](#)

Example of a board history file