

Documentation and LLCUs

Documentation/Wiki

- Wiki contains (almost) everything and allows interaction with the content
Among others you can find here:
 - All documents (user, design...)
 - Production manual
 - Boards' history files and bug reports
 - Link to shared drive containing all schematics
- Currently it is hosted by SDD wiki (TWiki), waiting for IT decision on a more suitable place
- Access is restricted
- If you feel you need access to it send an email to ngc@eso.org



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NGC

Welcome to the home of SDD.NGC. This is a web-based collaboration area for NGC

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[Hardware](#)

[Software](#)

[Link to the Official NGC Web Site](#)

[NGC Systems](#)

Site Tools of the NGC Web

- (More options in [WebSearch](#))
- [WebChanges](#): Display recent changes to the NGC web
- [WebIndex](#): List all NGC topics in alphabetical order. See also the faster [WebTopicList](#)
- [WebNotify](#): Subscribe to an e-mail alert sent when something changes in the NGC web
- [WebStatistics](#): View access statistics of the NGC web
- [WebPreferences](#): Preferences of the NGC web ([TWikiPreferences](#) has site-wide preferences)

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[KMOS](#)

[SPHERE](#)

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[ZIMPOL](#)

Last update: -- [AndreaBalestra](#) - 14 Jul 2008

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SDD > NGC > NgcSystems > **KMOS**

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KMOS final NGC-system, which is estimated to be delivered on **APRIL 2008**, contains the following modules:

<u>Module name</u>	<u>Serial number</u>	<u>Revision</u>	<u>Location</u>
Backplane	Backplane SN 12	3	ESO-Garching
Front End Basic	FEB SN 12	4	ESO-Garching
FEB Transition	FEB Trans 11	3	ESO-Garching
AQ-32CH	AQ-32 SN 10	3	ESO-Garching
AQ-32CH	AQ-32 SN 11	3	ESO-Garching
AQ-32CH	AQ-32 SN 15	3	ESO-Garching
AQ-32CH Transition	AQ-32 Trans 12?	3	ESO-Garching
AQ-32CH Transition	AQ-32 Trans 13?	3	ESO-Garching
AQ-32CH Transition	AQ-32 Trans 14?	3	ESO-Garching

Topic KMOS . { [Edit](#) | [Attach](#) | Backlinks: [Web](#) [All webs](#) | [Printable](#) | [History: r3 < r2 < r1](#) [More](#) }

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SDD > NGC > HardWare > NGCBackplane > History_Backplane > **Backplane_BoardNr12**

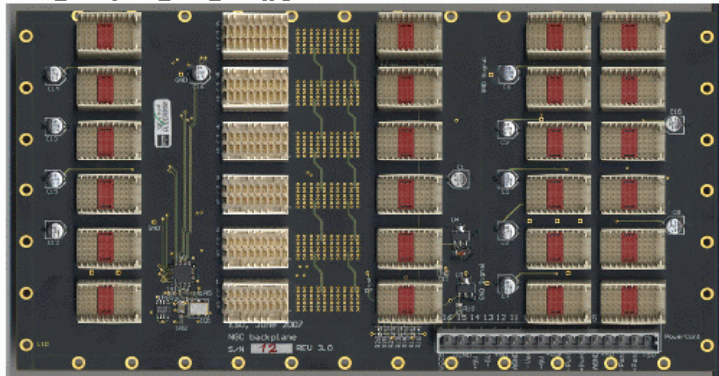
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board SN: #12

The following changes have been done:

- C2 has been replaced by a 3.3V zener diode.
- NGC_Backplane_rev3_12B.jpg

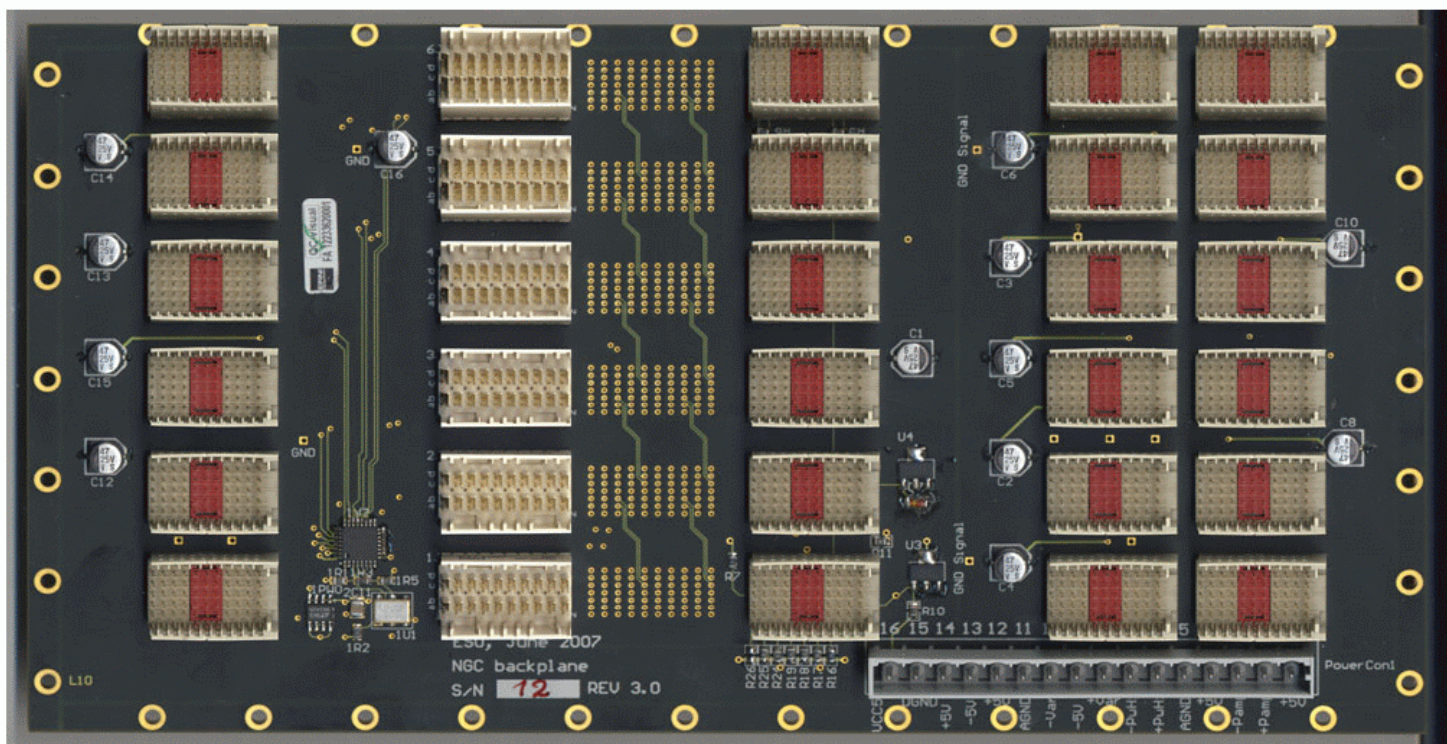


Attachment	Action	Size	Date	Who	Comment
NGC_Backplane_rev3_12B.jpg	manage	142.0 K	27 Sep 2007 - 11:50	LeanderMehrgan	

Topic Backplane_BoardNr12 . { [Edit](#) | [Attach](#) | Backlinks: [Web](#) [All webs](#) | [Printable](#) | [History](#): r1 [More](#) }

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-- [AndreaBalestra](#) - 06 Jul 2007

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Boards

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- ♦ [AQ32CH](#)
- ♦ [AQ32CH Transition Board](#)
- ♦ [CCD Preamp](#)
- ♦ [FEB](#)
- ♦ [FEB Transition Board](#)
- ♦ [NGC Backplane](#)
- ♦ [PCI Backend](#)
- ♦ [Test Tool Video](#)

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```
user_pref("capability.policy.policynames", "localfilelinks");
user_pref("capability.policy.localfilelinks.sites", "http://websqa.hq.eso.org");
user_pref("capability.policy.localfilelinks.checkloaduri.enabled", "allAccess");
```

to the user.js file located in your app directory (should be stg. like C:\Documents and Settings\put_your_username_here\Application Data\Mozilla\Firefox) If the user.js file does not exist, create it. More details can be found [here](#)

http://websqa.hq.eso.org/sdd/bin/view/NGC/AQ32CH



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-- [JavierReyes](#) - 06 Nov 2007

Topic AQ32CH . ([Edit](#) | [Attach](#) | Backlinks: [Web](#) [All webs](#) | [Printable](#) | [History: r2](#) < [r1](#) [More](#))

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- ◆ [Bugs_AQ32_Revision 1?](#)
- ◆ [Bugs_AQ32_Revision 2](#)
- ◆ [Bugs_AQ32_Revision 3](#)

-- [JavierReyes](#) - 17 Aug 2007

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AQ32 Rev.3.0 BUGS

- 1. The footprint for U15 (the offset DAC LT1206) is a little bit too big. It must be a 16-Lead Plastic SSOP (Narrow .150 Inch).
- 2. The exposed pad for the big voltage regulator is wrong (VR6,VR1, VR2 and VR5)
- 3. On LED DS1, it is better to have the LED always on after DONE-DUT. For that use a Tiny-Logic AND-gate instead of an NAND-gate.
- 4. The resistors R5, R20 and R21 must right after U2 and before SJ6 and SJ7. When the jumpers SJ6 and SJ7 are open SYS_CLK comes from the backplane and these resistors attenuate too much the signal. However, when the board is tested in standalone, the resistor are needed so U2 generates the clock.
- 5. Signals CONVERT_TO_BP, CONVERT_TO_BP#, CONVERT1_TO_BP and CONVERT1_TO_BP# are not connected to connected J3. I have temporarily connected CV1 and CV1# to pins B22, C22 respectively (GPIO3, GPIO4) on the FPGA.
- 6. Signals CONVERT1_TO_BP and CONVERT1_TO_BP# are not connected to connected J3. They are floating and that's the reason why the LED Busy on the front-panel is always on.
- 7. **This is not a bug.** Change U11. From 74ALS04 to 74F04 (cleaner convert signal on the oscilloscope)
- 8. **This is not a bug.** Signal EN_OUT_LEMO going to Monitor_Grouping_SchDoc is not connected.
- 9. **This is not a bug.** To improve the span of the offset correction the voltage reference U5 (ADR421, 2.5V) should be changed to the ADR444BRZ (4.096V).
- 10. The (+) and (-) outputs of the monitoring are swapped on the front panel. This is so because VIDEO_POS_FB and VIDEO_NEG_FB (outputs of U16 and inputs to U17 are swapped). This can be easily fixed by swapping the labels (+) and (-) on the front-panel.
- 11. Pins 32 and 33 are floating on 17U12, 18U12, 19U12, 20U12, 26U12, 27U12, 28U12, 29U12. These pins are Reset and /CS (pins 32 & 33 on the ADC). These pins must be connected to ground. The easiest is to connect the pins to the pins PD (Powerdown, pin 34 on the ADC).
- 12. The polarity sign of C115 and C116 is wrong. Minus and plus pin should be changed (Imehrgan).
- 13. Channel labels of all ADC channels on the PCB layout are wrong and should be ignored (Imehrgan).

POPULATION ERRORS

- 1. [POPULATION ERROR] The footprint for the LED DS1 is 0805 instead of 1206

- 8. **This is not a bug.** Signal EN_OUT_LEMO going to Monitor_Grouping_SchDoc is not connected.
- 9. **This is not a bug.** To improve the span of the offset correction the voltage reference U5 (ADR421, 2.5V) should be changed to the ADR444BRZ (4.096V).
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- 12. The polarity sign of C115 and C116 is wrong. Minus and plus pin should be changed (Imehrgan).
- 13. Channel labels of all ADC channels on the PCB layout are wrong and should be ignored (Imehrgan).

POPULATION ERRORS

- 1. [POPULATION ERROR] The footprint for the LED DS1 is 0805 instead of 1206.
- 2. [POPULATION ERROR] U7 should be the NC7S08M5 from FIERA stock (location 1594).
- 3. [POPULATION ERROR] R16 should not be populated because we always remove it to take the FPGA out of power-down.
- 4. [POPULATION ERROR] LEMO connector MonConvert should not be populated.
- 5. [POPULATION ERROR] VR1 and VR2 should be LT1963EQ-2.5 and they have populated the board with the LT1963EQ instead.
- 6. [POPULATION ERROR] U11 should be a 74F04 (from FIERA stock) to have a sharper signal on the CONVERT_LEMO connector.
- 7. [POPULATION ERROR] U5 could be changed to ADR444BRZ (4.096V reference).
- 8. [POPULATION ERROR] The text on the front-panel for the AQ32 is engraved. Tell CAD-Service to print it because is cheaper.
- 9. [POPULATION ERROR] For VR1, VR2, VR5 and VR6 use the regulator with the exposed pad cut.

-- [JavierReyes](#) - 17 Aug 2007

Topic [Bugs_AQ32_Revision3](#) . ([Edit](#) | [Attach](#) | Backlinks: [Web](#) [All webs](#) | [Printable](#) | [History](#): r13 < r12 < r11 < r10 < r9 [More](#))

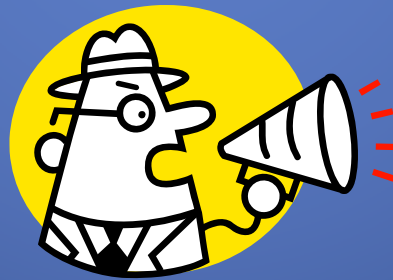
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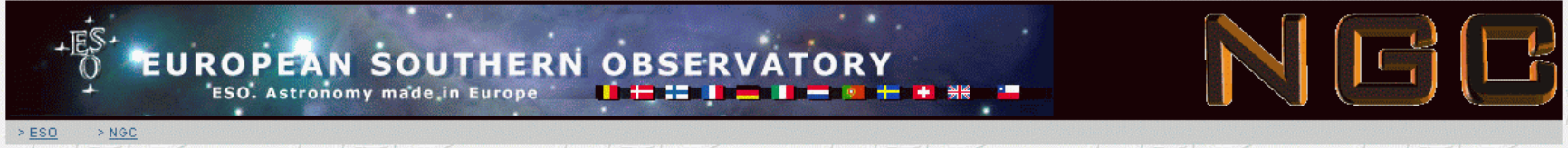


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Documentation/web

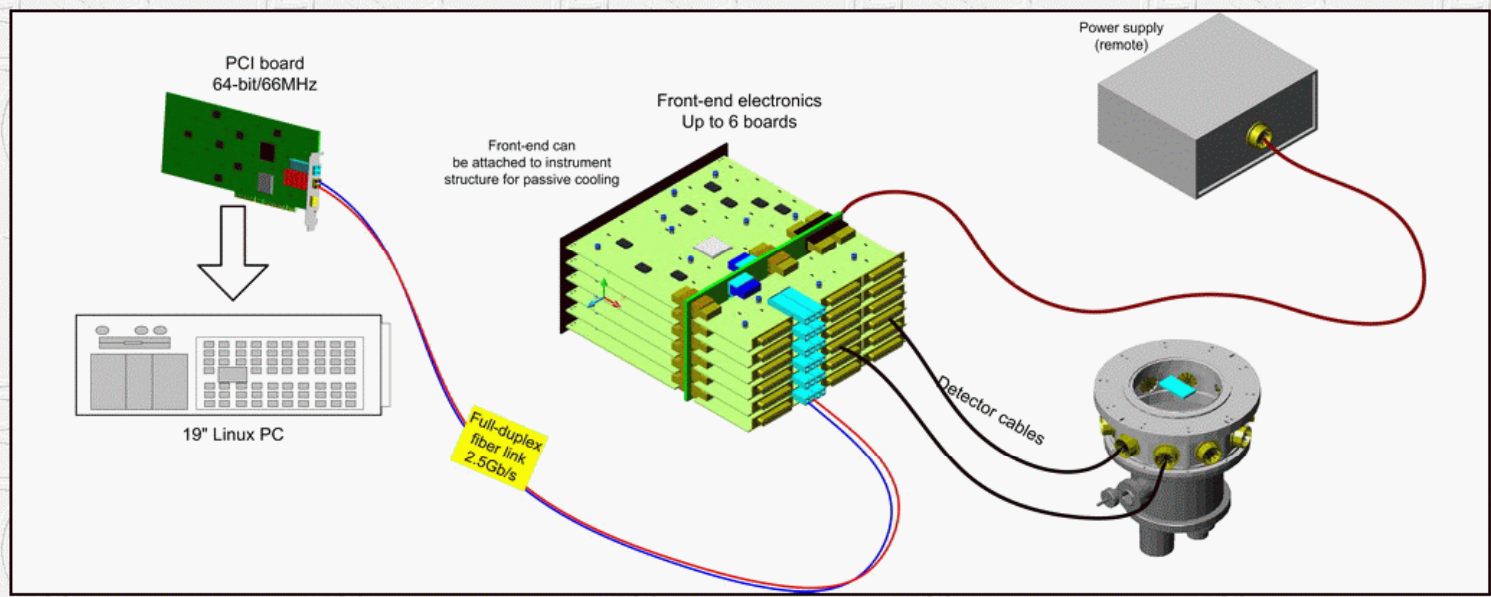
- Web (<http://www.eso.org/projects/ngc>) contains all public documents
- It is not foreseen as a maintenance tool, but as a mean to inform about NGC





New General Detector Controller

- [Introduction](#)
- [News](#)
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- [Tests](#)



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NGC



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> ESO > NGC

New General Detector Controller

Introduction

The name **New General detector Controller (NGC)** is the mission statement for this project:
"Provide a detector controller with capabilities that are a superset of both [FIERA](#) (= ESO's standard controller for CCDs) and [IRACE](#) (= ESO's default controller for infrared arrays)."

For the detector systems of future ESO instruments NGC will replace both of its predecessors. It is not currently planned to phase out any of the IRACE and FIERA systems deployed at the La Silla Paranal Observatory because they are performing well. The first instruments to be equipped with NGC systems will be [KMOS](#), [ZIMPOL](#) and [MUSE](#).

In addition to scientific imaging an application of growing importance will be fast signal sensing. This consists mainly of wavefront sensing for adaptive optics, the first applications being [GALACSI](#) on [MUSE](#), [GRAAL](#) on [HAWK-I](#) and [SAXO](#) on [SPHERE](#). Autoguiding and slow wavefront sensing for active optics will continue to be performed with [Technical CCDs \(TCCDs\)](#) or New-Generation Technical CCDs (NGTCCDs) and commercial controllers.

Details of the aimed-for capabilities are compiled in the *Requirements Document*. Various other documents reflect the evolution of both [Hardware](#) and [Software](#).

NGC is a joint project of the [Infrared Detector Department \(IDD\)](#) and the [Optical Detector Team \(ODT\)](#).

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> ESO > NGC

New General Detector Controller

Hardware

Documents

- ◆ **New General Detector Controller (NGC) - User Manual** (pdf-file, 2.7 MB)
ESO-Doc. No. VLT-MAN-ESO-13660-4510 by [M. Meyer et al.](#) (Jan/18/2008)
- ◆ **Interface Control Document for the New General Detector Controller (NGC)** (pdf-file, 490 kB)
ESO-Doc. No. VLT-ICD-ESO-13660-4009 by [M. Meyer et al.](#) (Feb/20/2007)

Papers

- ◆ **NGC - Detector Array Controller based on High Speed Serial Link Technology** (pdf-file, 110 kB)
Paper for SDW 2005 in Taormina (Italy) by [M. Meyer et al.](#) (Dec/05/2005)
- ◆ **NGC Front-End for CCDs and AO Applications** (pdf-file, 150 kB)
Paper for SDW 2005 in Taormina (Italy) by [J. Reyes et al.](#) (Jun/24/2005)

Presentations

- ◆ **NGC and L3 CCDs** (pdf-file, 820 kB)
Presentation of NGC "first light" with L3 CCDs by [M. Meyer](#) (Dec/05/2005)
- ◆ **NGC - Detector Array Controller based on High Speed Serial Link Technology** (pdf-file, 1.1 MB)
Presentation of NGC "first light" with PICNIC array by [M. Meyer](#) (Dec/05/2005)
- ◆ **CCD head for AO** (pdf-file, 710 kB)
Presentation at ESO by [J. Reyes](#) (Dec/08/2004)

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NGC LLCUs (Linux Local Control Units)

- LLCUs are standard Linux machines as defined by SDD in: <http://websqa.hq.eso.org/sdd/bin/view/SDDInfo/LinuxStandardHw>
- NGC team takes care of verifying upfront that the standard models covers minimum NGC requirements:
 - 2 x 3.00GHz CPU (4 MB cache) for real parallel processing
 - 2GB Memory
 - 2 Full-width PCI slots (64 Bit 66 Mhz)
 - Gigabit Ethernet
 - Graphic Card for maintenance operations. No special requirement.
 - Hard Disk >160 GB, i.e. capable of some local storage for testing purposes (given an upper limit of occupation of operating system + VLTSW of 10 GB).
 - Rack mountable
 - Dimension compatible with rack requirements as defined by TEC.
 - Safe under the applicable earthquake conditions

LLCUs location

- It is technically possible to have the LLCUs either close to the instrument (e.g. Nasmyth platform) or in the Computer Room.
- CRE N. VLT-CRE-ESO-13660-4412 (asking for a formal acceptance of LLCUs in Computer Room was rejected but somehow accepted (!):
 - Rejected as CRE
 - Accepted the concept: each project can ask for relocation of LLCU(s) in the Computer Room